

HS6230 RF Register Map

Version 0.9

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Revision History

Revision	Date	Description
V0.1	2019-4-11	Initial version
V0.2	2019-7-1	Update some registers
V0.3	2019-7-3	Add bp_pd_osc32k
V0.4	2019-7-19	Update SETUP_AW and SETUP_VALUE
V0.5	2019-7-21	Update CAL_DONE
V0.6	2019-8-6	Update reset method of CAL_DONE
V0.7	2019-12-9	Add some guideline for RF mode
V0.8	2019-12-12	Update some guideline for RF mode
V0.9	2020-7-26	Update SETUP_AW

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Register Definition

BANK0

CONFIG (RW) Address: 00h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	MASK_RX_ DR	MASK_TX_ DS	MASK_MA X_RT	EN_CRC	CRCO	PWR_UP	PRIM_RX
0	0	0	0	1	0	1	0
RW	RW	RW	W	RW	RW	RW	RW

SETUP_AW (RW) Address: 03h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDU TYPE				RxAdd	TxAdd	SETUP_AW	
4b'0010				0	0	2'b11	
RW				RW	RW	RW	

Note: PDU TYPE only support 0010 ADV_NONCONN_IND

RF_CH (RW) Address: 05h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reg_Rf_ch							
8'h32							
RW							

RF_SETUP (RW) Address: 06h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CONT_WAV E	PA_PWR[3]	RF_DR_LO W	Reserved	RF_DR_HIG H	Pa_power		
0	0	0	0	0	3'b101		
RW	RW	RW	RW	RW	RW		

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STATUS (RW) Address: 07h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BANK	Reserved	TX_DS	Reserved	Reserved			TX_FULL
0	0	0	0	3'b000			0
R	RW	RW	RW	R			R

KEY_VALUE Address: 08h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
KEY_VALUE2				KEY_VALUE1			
4'h0				4'h0			
R				R			

PRE_LEN (RW) Address: 09h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Preamble_length							
8'h0							
RW							

TX_ADDR(RW) Address: 10h

Bit 47	Bit 46	Bit 45	Bit 44	Bit 43	Bit 42	Bit 41	Bit 40
TX_ADDR							
8'h6b							
RW							
Bit 39	Bit 38	Bit 37	Bit 36	Bit 35	Bit 34	Bit 33	Bit 32
TX_ADDR							
8'h6b							
RW							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
TX_ADDR							
8'h7d							
RW							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
TX_ADDR							
8'h91							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

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TX_ADDR							
8'h71							
RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX_ADDR							
8'h46							
RW							

FIFO_STATUS (RW) Address: 17h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	TX_REUSE_PL	TX_FULL	TX_EMPTY	Reserved		Reserved	Reserved
0	0	0	1	0		0	0
RW	R	R	R	RW		R	R

RPD_0 (R) Address: 18h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved			reservrd	cal_st_cs			
000			0	0			
R			R	R			

FEATURE (RW) Address: 1Dh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved			bp_pd_osc32k	bp_pd_rc2m	EN_DPL	Reserved	Reserved
0			0	0	0	0	0
RW			RW	RW	RW	RW	RW

SETUP_VALUE (RW) Address: 1Eh

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
REG_MBG_WAIT							
8'h06							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
TX_SETUP_VALUE							
8'h32							

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RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				CE_REG	BLE_EN	KEY_EN	CAL_DONE
0				0	0	1	0
RW							

Note:

Bit3=CE_REG, default 0, CE=P0.0||(CE_REG), when pull down of P0.0 is enabled, CE_REG can be used to control CE,

Bit2=BLE_EN, default 0, when BLE_EN=1, 6230 transmits ble broadcast packet,

Bit1=KEY_EN, default 1, when KEY_EN=0, KEY1, KEY2 and wake up is disabled,

Bit0=CAL_DONE, default 0, after calibration done, CAL_DONE=1, when writing CAL_EN=1, CAL_DONE will be reset.

PRE_GURD (RW) Address: 1Fh

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
SPARE_REG[15:8]							
0							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
SPARE_REG[7:0]							
0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TAIL_CTL			GRD_EN	GRD_CNT			
3'h3			1	4'h7			
RW			RW	RW			

Bank1

LINE (R) Address: 00h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
CID							
8'h05							
R							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CID							
8'h70							
R							

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PLL_CTL0 (RW) Address: 01h

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Soft_rst	Reserved	Reserved	Cry_pd_reg	Cry_pd_mn	Reserved	tx_buf_bp	Reserved
0	0	0	0	0	0	1	0
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Reserved	Bp_dac	Bp_afc	Reserved	bp_vco_ldo	Vco_ldo_cal_reg		
0	0	0	0	0	0		
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Vco_ldo_cal_mn	Reserved	Reserved					Reserved
0	0	0					0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	CAL_EN	PLL_FOFFSET_SEL		DAC_CALM ODE_REG	DAC_RANG E_MN
0	0	0	1	01		0	0

FAGC_CTRL (RW) Address: 03h

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit24
Reserved							gard_en
0							1
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Pa_cm		Reserved		pa_cas_ctl		scramble_en	Reserved
0	0	0		1	0	1	0
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved							
0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved					Bm_xtal	Xtal_resc	
0					1	00	

TEST_PKDET (RW) Address: 05h

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit24
test_en	psudo_rnd	test_pat_en	Reserved	Reserved	Reserved	Reserved	Reserved
0	0	0	0	0	0	0	0
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
test_mode			test_point_sel1			test_point_sel0	
0	0	0	0	0	0	0	0

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Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved							
0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Pd_pa_reg	Pd_pa_mn	Pa_voltage	Xtal_cc				
0	0	0	1	1	1	1	1

PLL_CTRL_1 (RW) Address: 06h

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Reserved	afc_w_sel		doc_dac_mn	pd_pll_mn	pd_pll_reg	ftuning_mn	ctuning_mn
0	1	1	0	0	0	0	0
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
reg_tx_pa_wait							
0	0	0	1	0	0	0	0
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
tx_pll_wait							
0	1	0	0	0	0	1	0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reg_afc_wait							
0	0	0	0	0	0	0	0

STATUS (RW) Address: 07h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
bank		state_cs					
0	0	0					
RW		R					

CTUNING (RW) Address: 08h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved			CTUNING_REG_TX				
0			0				
R			RW				

FTUNING (RW) Address: 09h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved					FTUNING_REG_TX		

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0	
R	RW

FDEV (RW) Address: 0ch

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	FDEV						
0	8'h20						
R	RW						

DAC_RANGE (RW) Address: 11h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	DAC_RANGE_REG						
0	0						
R	RW						

CHAN (RW) Address: 12h

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Chan_mn	Reserved	CHAN_FRAC_REG					
0	0	0					
RW	RW	RW					
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
CHAN_FRAC_REG							
0							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
CHAN_FRAC_REG							CHAN_INT_REG
0							0
RW							RW
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHAN_INT_REG							
0							
RW							

RF configuration guideline of 1Mbps

上电校准:

SPI_RF 模式，上电后要 delay 10ms，待 6230 完成上电复位，再进行上电校准，TX_ASIC 模式忽略这一步；

无需配置任何寄存器，直接给 CE pulse，即可启动上电校准，SPI_RF 模式下，CE pulse 通过写 CE_REG 来实现，CE_REG 在 bank0 的 **SETUP_VALUE** 寄存器的 bit3，操作方式跟 6200 一致；

上电校准启动后，可以通过查询 CAL_DONE 寄存器来判断校准是否执行完毕，CAL_DONE 寄存器在 bank0 的 SETUP_VALUE 寄存器的 bit0，默认值是 0，读到 1 表示校准完成，再次校准时可以通过写 CAL_EN=1 去完成对 CAL_DONE 清零；

休眠后校准值会丢失，所以第一次上电校准后，需要把校准值记录到 RF 寄存器中，需要记录 **DAC_RANGE** 和 vco_ldo_cal_reg，然后把 vco_ldo_cal_mn 和 DAC_RANGE_MN 都置 1（vco_ldo_cal_reg、vco_ldo_cal_mn 和 DAC_RANGE_MN 都在 bank1 的 PLL_CTL0 里），这样每次唤醒后就不用执行校准了；

初始化:

配置 Bank1 的 **PLL_CTL0**，bit7~0=0x07， bit15~8=0x80， bit23~16=0x48；

CONFIG、RF_CH、RF_SETUP、TX_ADDR 和 FEATURE 寄存器，根据应用去配置；

需要注意 6230 的 STATUS 寄存器与 6200 不同，6200 在 bank0 和 bank1 中都有 STATUS 寄存器且功能一样，6230 在 bank1 中的 STATUS 寄存器只能切 bank 用，如果要查询 TX_DS 和 TX_FULL 必须用 bank0 的 STATUS 寄存器；

Bank0 中新增了 **KEY_VALUE** 寄存器，用来存按键值，TX_ASIC 模式软件也读这个寄存器；

6230 如果工作在 1Mbps，配置 RF 的时候只需操作上述 9 个寄存器。

注意事项:

1. RF 模式从休眠状态唤醒（CONFIG 寄存器中的 PWR_UP 写 1）后，晶振需要大约 2.8ms 才能启动，为了应用的可靠性，建议软件 **延迟 4ms 等晶振启动**；
2. 等待晶振启动期间，不能操作 CE，否则芯片会死机，需要延迟 4ms 之后才能拉 CE；
3. 等待晶振启动期间，不能写 TX FIFO，需要延迟 4ms 之后才能写 TX FIFO；
4. 等待晶振启动期间，如果不是特别在意功耗的应用，建议尽量不要读写寄存器（不是强制规定）；
5. RF 模式进入休眠（CONFIG 寄存器中的 PWR_UP 写 0）后，数字 LDO 会有一个降低再升高的建立过程，这段时间内不要操作 SPI，延迟 1ms 后才进行操作；
6. RF 模式进入休眠之后，除了写 CONFIG 寄存器进行唤醒之外，建议尽量不要操作 SPI（不是强制规定）；

7. RF 模式如果不用 6230 的按键 (P06 和 P07), 一定要把 KEY_EN 关掉, 在 SETUP_VALUE 中把 bit1 置 0;
8. 上电校准完成后, CAL_DONE 寄存器会变为 1, 如果要把这个寄存器清 0, 需要把 CAL_EN 写 1;
9. 6230 RF 模式的上电校准可以不像 6200 那样延迟 40ms 等待校准完成, 通过查询 CAL_DONE 寄存器可以判断校准是否完成;