

OTP-Based 8-Bit Microcontroller

Devices Included in this Data Sheet:

- FM8PE531MA: 14-pin OTP device
- FM8PE531MB: 16-pin OTP device

GENERAL DESCRIPTION

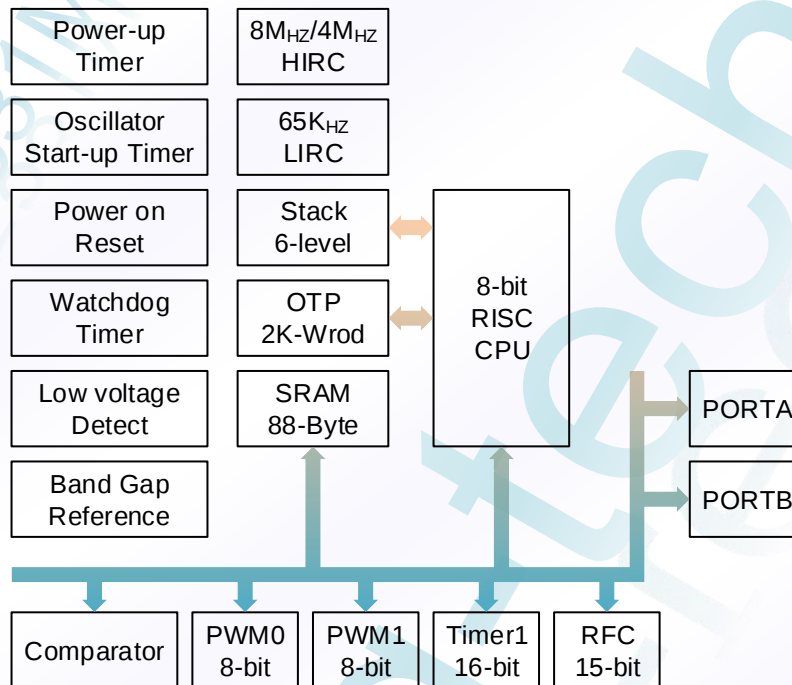
The FM8PE531M is a low-cost, high speed, high noise immunity, OTP-based 8-bit CMOS microcontrollers. It employs a RISC architecture with only 37 instructions. All instructions are single cycle except for program branches which take two cycles. The easy to use and easy to remember instruction set reduces development time significantly.

The FM8PE531M consists of Power-on Reset (POR), Brown-out Reset (BOR), Power-up Reset Timer (PWRT), Watchdog Timer, OTP, SRAM, tristate I/O port, I/O pull-high control, Power saving SLEEP mode, real time programmable clock/counter, Interrupt, PWM, Comparator (with CV_{REF} , Fixed Band Gap reference voltage), Wake-up from SLEEP mode, and Code Protection for OTP products.

FEATURES

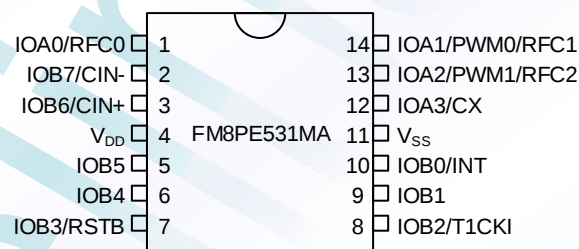
- 2K Word on chip OTP-ROM and 88 Bytes on chip general purpose registers (SRAM).
- 6-level deep hardware stack.
- One analog comparator.
 - Internal reference voltage: 16-step CV_{REF} module, 1.2V fixed voltage reference.
- One 16-bit real timer/Counter with 2-bit programmable pre-scaler.
- Two 8-bit fixed period-cycle PWM.
- Three channel 15-bit RFC.
- Six levels LVDT (Low Voltage Detect): 3.6V, 2.6V, 2.4V, 2.2V, 2.0V and 1.8V.
- Power-up Reset Timer (PWRT)
- On chip Watchdog Timer (WDT) with internal oscillator for reliable operation.
- Two I/O port, PORTA and PORTB with independent direction control:
 - 13 Bi-direction I/O pin (Programmable Pull-up enable in Input mode).
 - One Input /Open-drain pin (IOB3/RSTB).
- Two kinds of interrupt source:
 - 4 internal interrupt sources: Timer1, RFC, Comparator and LVDT.
 - 1 external interrupt sources: INT pin.
- Wake-up from SLEEP:
 - ALL pin (IOA0~IOA5, IOB0~IOB7) change wakeup.
 - WDT overflow.
- Power saving SLEEP mode.
- Programmable Code Protection.
- Selectable oscillator options:
 - HIRC: Internal Resistor/Capacitor 8MHz/4MHz Oscillator.
 - LIRC: Internal Resistor/Capacitor 65KHz Oscillator.
- Wide-operating voltage range: 2.0V to 5.5V.

BLOCK DIAGRAM

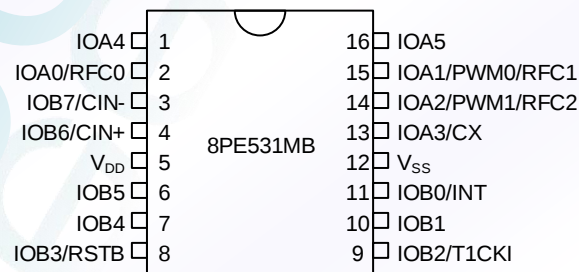


PIN CONNECTION

DIP/SOP14



DIP/SOP16



PIN DESCRIPTIONS

Name	I/O	Description
IOA0/RFC0	I/O	• Bi-direction I/O port with wake-up function (programmable Pull-high in Input mode). • The RC oscillator network output0 of RFC module.
IOA1/PWM0/RFC1	I/O	• Bi-direction I/O port with wake-up function (programmable Pull-high in Input mode). • PWM0 output. • The RC oscillator network output1 of RFC module.
IOA2/PWM1/RFC2	I/O	• Bi-direction I/O port with wake-up function (programmable Pull-high in Input mode). • PWM1 output. • The RC oscillator network output2 of RFC module.
IOA3/CX	I/O	• Bi-direction I/O port with wake-up function (programmable Pull-high in Input mode). • The RC oscillator network input of RFC module.
IOA4, IOA5 IOB1, IOB4, IOB5	I/O	• Bi-direction I/O port with wake-up function (programmable Pull-high in Input mode).
IOB0/INT	I/O	• Bi-direction I/O port with wake-up function (programmable Pull-high in Input mode). • External interrupt input.
IOB2/T1CKI	I/O	• Bi-direction I/O port with wake-up function (programmable Pull-high in Input mode). • External clock input to Timer1.
IOB3/RSTB	I/O	• Input pin only with system wake-up/pin change interrupt function; voltage on this pin must not exceed V_{DD}. • System clear (RESET) input. This pin is an active low RESET to the device. • Open-Drain output.
IOB6/CIN+	I/O	• Bi-direction I/O port with wake-up function (programmable Pull-high in Input mode). • Comparator positive input.
IOB7/CIN-	I/O	• Bi-direction I/O port with wake-up function (programmable Pull-high in Input mode). • Comparator negative input.
V _{DD}	-	Positive supply.
V _{SS}	-	Ground.

Legend: I=input, O=output, I/O=input/output.

1.0 MEMORY ORGANIZATION

FM8PE531M memory is organized into program memory and data memory.

1.1 Program Memory Organization

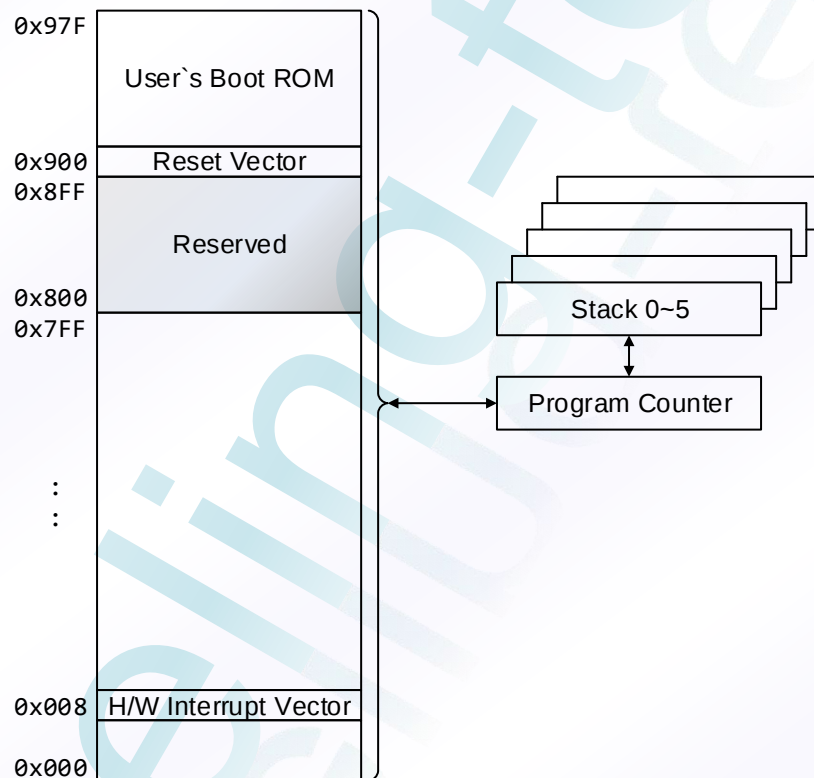
The FM8PE531M have a 12-bit Program Counter capable of addressing a 2K program memory space.

The RESET vector for the FM8PE531M is at 0x900.

The H/W interrupt vector is at 0x008.

CALL and GOTO instructions only have a 10-bit address range. This 10-bit address range allows a branch within a 1K program memory page size. To allow CALL and GOTO instructions to address the entire 2K program memory address range for 8PE531M, there is other two bits to specify the program memory page. This paging bit comes from the PG<1:0> bits (STATUS<6:5>, STATUS<6> must keep 0.).

Figure 1.1: Program Memory Map and STACK



1.2 Data Memory Organization

Data memory is composed of Special Function Registers and General Purpose Registers.

The General Purpose Registers are accessed either directly or indirectly through the FSR register.

The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device.

In FM8PE531M, the data memory is partitioned into four banks. Switching between these banks requires the RP1, RP0 bits in the FSR register to be configured for the desired bank.

Table 1.1: Registers File Map for FM8PE531M

FSR<7:6> Address	Description			
	0 0 Bank 0	0 1 Bank 1	1 0 Bank 2	1 1 Bank 3
0x00	INDF			
0x02	PCL			
0x03	STATUS			
0x04	FSR			
0x05	IOSTA			
0x06	PORTA			
0x07	IOSTB			
0x08	PORTB			
0x09	T1CON			
0x0A	TMR1LB			
0x0B	TMR1HB			
0x0C	OSCCON			
0x0D	LVDTCON			
0x0E	INTEN			
0x0F	INTFLAG			
0x10	PWMCON		AWUCON	
0x11	P0DPR		APHCON	
0x12	P1DPR		BWUCON	
0x13	RFCCON		BPHCON	
0x14	RFCDLB		CMPCON1	
0x15	RFCDHB		CMPCON2	
0x18 0x2F	General Purpose Registers	Memory back to address in Bank 0		
0x30 0x3F	General Purpose Registers	General Purpose Registers	General Purpose Registers	General Purpose Registers

Table 1.2: Operational Registers Map

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
Unbanked									
0x00 (r/w)	INDF	Uses contents of FSR to address data memory (not a physical register)							
0x02 (r/w)	PCL	Low order 8 bits of PC							
0x03 (r/w)	STATUS	RST	PG1	PG0	T0	PD	Z	DC	C
0x04 (r/w)	FSR	RP1	RP0	Indirect data memory address pointer					
0x05 (r/w)	IOSTA	-	-	IOSTA5	IOSTA4	IOSTA3	IOSTA2	IOSTA1	IOSTA0
0x06 (r/w)	PORTA	-	-	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0
0x07 (r/w)	IOSTB	IOSTB7	IOSTB6	IOSTB5	IOSTB4	IOSTB3	IOSTB2	IOSTB1	IOSTB0
0x08 (r/w)	PORTB	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0
0x09 (r/w)	T1CON	-	-	-	T1PS1	T1PS0	GP	T1CS	T1EN
0x0A (r/w)	TMR1LB	Low byte of 16-bit real-time clock/counter 1							
0x0B (r/w)	TMR1HB	High byte of 16-bit real-time clock/counter 1							
0x0C (r/w)	OSCCON	WDTEN	IRCN	WDTSEL1	WDTSEL0	CPUS	IRCF2	IRCF1	IRCF0
0x0D (r/w)	LVDTCN	EIS	RDPORT	IOB3EN	LVREN	INTEDG	LVDSSEL2	LVDSSEL1	LVDSSEL0
0x0E (r/w)	INTEN	GIE	-	-	LVDTIE	CMPIE	INTIE	RFCIE	T1IE
0x0F (r/w)	INTFLAG	-	-	-	LVDTIF	CMPIF	INTIF	RFCIF	T1IF
Bank0, 1									
0x10 (r/w)	PWMCON	-	-	-	PWMCS2	PWMCS1	PWMCS0	P1EN	P0EN
0x11 (r/w)	P0DPR	PWM0 Duty Compare Pre-set register							
0x12 (r/w)	P1DPR	PWM1 Duty Compare Pre-set register							
0x13 (r/w)	RFCCON	RFCN	START	-	RFCMOD	-	-	RFCS1	RFCS0
0x14 (r)	RFCDLB	Low byte of 15 bit RFC conversion result							
0x15 (r)	RFCDHB	RFCOV	RFCD14	RFCD13	RFCD12	RFCD11	RFCD10	RFCD9	RFCD8
Bank2, 3									
0x10 (r/w)	AWUCON	-	-	WUA5	WUA4	WUA3	WUA2	WUA1	WUA0
0x11 (r/w)	APHCON	-	-	/PHA5	/PHA4	/PHA3	/PHA2	/PHA1	/PHA0
0x12 (r/w)	BWUCON	WUB7	WUB6	WUB5	WUB4	WUB3	WUB2	WUB1	WUB0
0x13 (r/w)	BPHCON	/PHB7	/PHB6	/PHB5	/PHB4	GP	/PHB2	/PHB1	/PHB0
0x14 (r/w)	CMPCON1	-	-	COUT	CINV	CINS	CM2	CM1	CM0
0x15 (r/w)	CMPCON2	-	-	CVREN	CVRR	CVR3	CVR2	CVR1	CVR0

Legend: - = unimplemented, read as '0'.

2.0 FUNCTIONAL DESCRIPTIONS

2.1 Operational Registers

2.1.1 INDF (Indirect Addressing Register)

Read/Write-POR		R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x00	INDF	Uses contents of FSR to address data memory (not a physical register)							

The INDF Register is not a physical register. Any instruction accessing the INDF register can actually access the register pointed by FSR Register. Reading the INDF register itself indirectly (FSR="0x00") will read 0x00. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected).

The bits 5-0 of FSR register are used to select up to 64 registers (address: 0x00 ~ 0x3F).

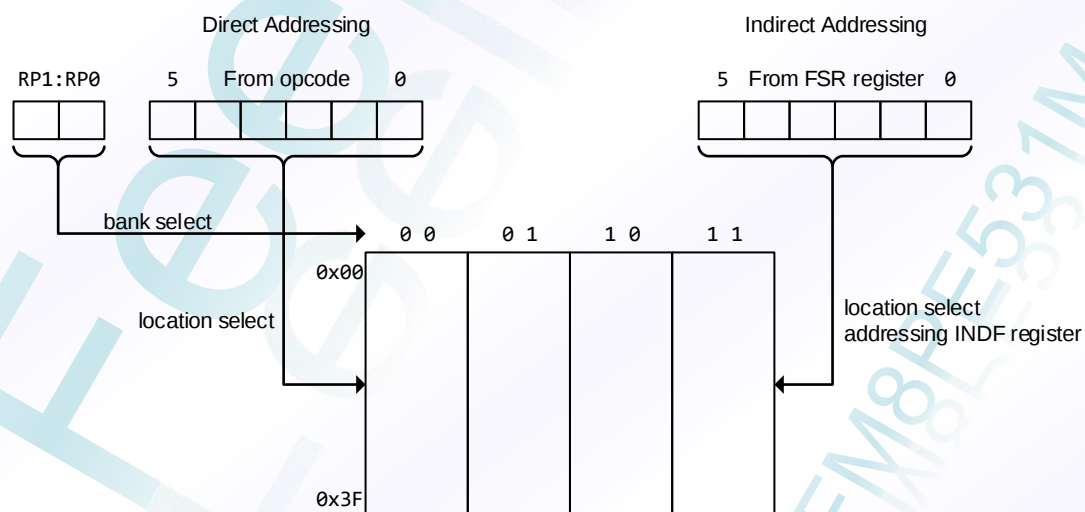
In FM8PE531M, the data memory is partitioned into four banks. Switching between these banks requires the RP1 and RP0 bits in the FSR register to be configured for the desired bank. The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers. All Special Function Registers and some of General Purpose Registers from other banks are mirrored in bank 0 for code reduction and quicker access.

RP1:RP0	Accessed Bank
0 0	0
0 1	1
1 0	2
1 1	3

Example 2.1: INDIRECT ADDRESSING

- Register file 0x18 contains the value 0x10
- Register file 0x19 contains the value 0x0A
- Load the value 0x18 into the FSR Register
- A read of the INDF Register will return the value of 0x10
- Increment the value of the FSR Register by one (@FSR=0x19)
- A read of the INDF register now will return the value of 0x0A.

Figure 2.1: Direct/Indirect Addressing



2.1.2 PCL (Low Byte of Program Counter) & Stack

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x02	PCL	Low order 8 bits of PC							

FM8PE531M devices have a 12-bit wide Program Counter (PC) and eight-level deep 12-bit hardware push/pop stack. The low byte of PC is called the PCL register. This register is readable and writable. The high byte of PC is called the PCH register. This register contains the PC<11:8> bits and is not directly readable or writable. All updates to the PCH register go through the PG<1:0> bits (STATUS<6:5>). As a program instruction is executed, the Program Counter will contain the address of the next program instruction to be executed. The PC value is increased by one, every instruction cycle, unless an instruction changes the PC.

For a GOTO instruction, the PC<9:0> is provided by the GOTO instruction word. The PC<11:10> is updated from the PG<1:0> bits (STATUS<6:5>). The PCL register is mapped to PC<7:0>.

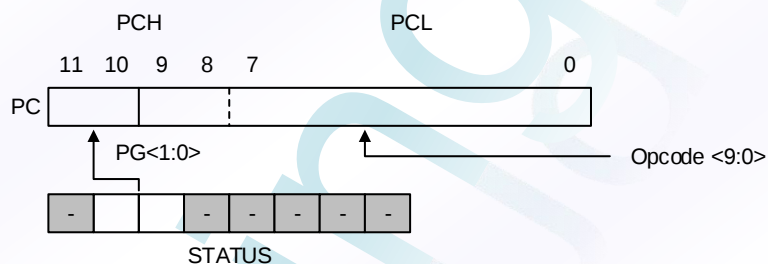
For a CALL instruction, the PC<9:0> is provided by the CALL instruction word. The PC<11:10> is updated from the PG<1:0> bits (STATUS<6:5>). The next PC will be loaded (PUSHed) into the top of STACK. The PCL register is mapped to PC<7:0>.

For a RETIA, RETFIE, or RETURN instruction, the PC are updated (POPed) from the top of STACK. The PCL register is mapped to PC<7:0>.

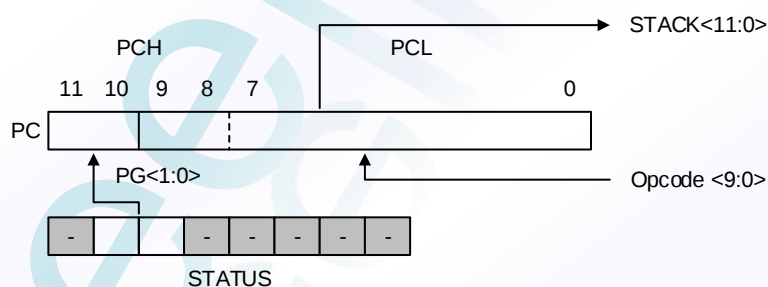
For any instruction where the PCL is the destination, the PC<7:0> is provided by the instruction word or ALU result.

Figure 2.2: Loading of PC in Different Situations

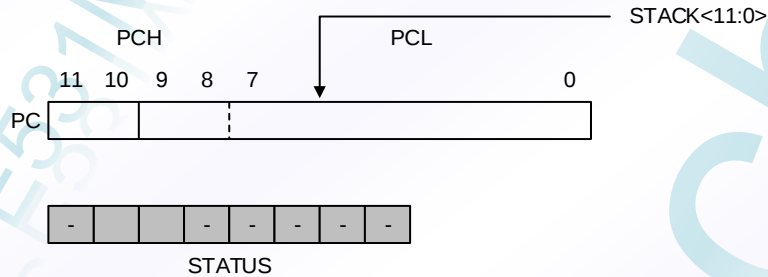
Situation 1: **GOTO** Instruction



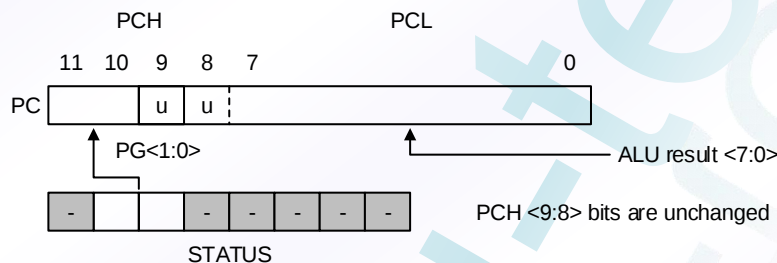
Situation 2: **CALL** Instruction



Situation 3: **RETIA**, **RETFIE**, or **RETURN** Instruction



Situation 4: Instruction with PCL as destination



2.1.3 STATUS (Status Register)

Read/Write-POR		R/W-0	R/W-1	R/W-0	R-#	R-#	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x03	STATUS	RST	PG1	PG0	T0	PD	Z	DC	C

Legend: # = refer Table 2.4 for detail description.

This register contains the arithmetic status of the ALU, the RESET status.

If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{T0}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended. For example, **CLRR STATUS** will clear the upper three bits and set the Z bit. This leaves the STATUS Register as 000u u1uu (where u = unchanged).

C: Carry/borrow bit.

ADDAR, ADDIA

= 0, No Carry occurred.

= 1, Carry occurred.

SUBAR, SUBIA

= 0, Borrow occurred.

= 1, No borrow occurred.

Note: A subtraction is executed by adding the two's complement of the second operand. For rotate (RRR, RLR) instructions, this bit is loaded with either the high or low order bit of the source register.

DC: Half carry/half borrow bit.

ADDAR, ADDIA

= 0, No Carry from the 4th low order bit of the result occurred.

= 1, Carry from the 4th low order bit of the result occurred.

SUBAR, SUBIA

= 0, Borrow from the 4th low order bit of the result occurred.

= 1, No Borrow from the 4th low order bit of the result occurred.

Z: Zero bit.

= 0, The result of a logic operation is not zero.

= 1, The result of a logic operation is zero.

PD: Power down flag bit.

= 0, by the SLEEP instruction.

= 1, after power-up or by the CLRWDI instruction.

TO: Time overflow flag bit.

= 0, a watch-dog time overflow occurred.

= 1, after power-up or by the CLRWDI or SLEEP instruction.

PG1:PG0: Program memory page select bits. Used for GOTO, CALL, or any instruction with PCL as destination.

PG1:PG0		Program Memory Page [Address]
0	0	Page 0 [0x000~0x3FF]
0	1	Page 1 [0x400~0x7FF]
1	0	Page 2 [0x900~0x97F]
1	1	Inhibit

Note: Page0 and 1 is User's main program area, page2 is User's Boot ROM.

RST: Bit for wake-up type.

= 0, Wake-up from other reset types.

= 1, Wake-up from SLEEP.

2.1.4 FSR (Indirect Data Memory Address Pointer)

Read/Write-POR		R/W-0	R/W-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x04	FSR	RP1	RP0	Indirect data memory address pointer					

Bit5:Bit0: Select registers address in the indirect addressing mode.

RP1:RP0: These bits are used to switching the bank of four data memory banks.

2.1.5 IOSTA & IOSTB (Port I/O Control Register)

Read/Write-POR	-	-	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x05	IOSTA	-	-	IOSTA5	IOSTA4	IOSTA3	IOSTA2	IOSTA1	IOSTA0

Read/Write-POR	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x07	IOSTB	IOSTB7	IOSTB6	IOSTB5	IOSTB4	IOSTB3	IOSTB2	IOSTB1	IOSTB0

Legend: - = unimplemented, read as '0'.

IOSTA5:IOSTA0: PORTA I/O control bit.

- = 0, PORTA pin configured as an output.
- = 1, PORTA pin configured as an input (tri-stated).

IOSTB7:IOSTB0: PORTB I/O control bit.

- = 0, PORTB pin configured as an output.
- = 1, PORTB pin configured as an input (tri-stated).
- Note: IOB3 is open-drain output only if IOSTB3 = 0.

2.1.6 PORTA & PORTB (Port Data Register)

Read/Write-POR	-	-	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x06	PORTA	-	-	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0

Read/Write-POR	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x08	PORTB	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0

Reading the port (PORTA and PORTB register) reads the status of the pins independent of the pin's input/output modes. Writing to these ports will write to the port data latch.

IOA5:IOA0: PORTA I/O pin.

- = 0, Port pin is low level.
- = 1, Port pin is high level.

IOB7:IOB0: PORTB I/O pin.

- = 0, Port pin is low level.
- = 1, Port pin is high level.
- Note: IOB3 is open-drain output only if IOSTB3 = 0.

2.1.7 T1CON (Timer 1 Control Register)

Read/Write-POR		-	-	-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x09	T1CON	-	-	-	T1PS1	T1PS0	GP	T1CS	T1EN

Legend: - = unimplemented, read as '0'.

T1EN: Timer1 Enable/Disable bit.

= 0, Disable Timer1.

= 1, Enable Timer1.

T1CS: Timer1 clock source select bit.

= 0, Internal instruction clock cycle.

= 1, External T1CKI pin.

GP: General purpose read/write bits.

T1PS1:T1PS0: Timer1 pre-scaler rate select bits.

T1PS1:T1PS0	Pre-scaler Rate
0 0	1:1
0 1	1:2
1 0	1:4
1 1	1:8

2.1.8 TMR1LB and TMR1HB (Timer 1 Clock/Counter Register)

Read/Write-POR		R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0A	TMR1LB	Low byte of 16-bit real-time clock/counter 1							

Read/Write-POR		R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0B	TMR1HB	High byte of 16-bit real-time clock/counter 1							

The Timer1 is a 16-bit timer/counter. The clock source of Timer1 can come from the instruction cycle clock or by an external clock source (T1CKI pin) defined by T1CS bit (T1CON<1>). If T1CKI pin is selected, the Timer1 is increased by T1CKI signal rising edge.

2.1.9 OSCCON (Oscillator Control Register)

Read/Write-POR		R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0C	OSCCON	WDTEN	IRCEN	WDTSEL1	WDTSEL0	CPUS	IRCF2	IRCF1	IRCF0

IRCF2:IRCF0: Internal RC oscillator frequency select bits.

IRCF2:IRCF0	Description
0 0 0	HIRC/1
0 0 1	HIRC/2
0 1 0	HIRC/4
0 1 1	HIRC/8
1 0 0	HIRC/16
1 0 1	HIRC/32
Other	No function, do not use.

CPUS: CPU clock source select bit.

= 0, CPU clock source is LIRC.

= 1, CPU clock source is HIRC, frequency defined by IRCF<2:0> bits.

WDTSEL1:WDTSEL0: Watchdog time-out select bits.

WDTSEL1:WDTSEL0	Time-out
0 0	2Sec
0 1	288mS
1 0	72mS
1 1	18mS

IRCEN: Internal RC enable bit

= 0, Disable internal RC clock source (Power down HIRC).

= 1, Enable internal RC clock source.

Note: Make sure the system clock (F_{cpu}) been switch to LIRC source before power down internal RC.

WDTEN: Watchdog Timer enable bit.

= 0, WDT Disable.

= 1, WDT Enable.

2.1.10 LVDTCON (LVDT Control Register)

Read/Write-POR		R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0D	LVDTCON	EIS	RDPORT	IOB3EN	LVREN	INTEDG	LVDSSEL2	LVDSSEL1	LVDSSEL0

LVDSSEL2:LVDSSEL0: Low voltage detects select bits.

LVDSSEL2:LVDSSEL0	Description
0 0 0	2.6V
0 0 1	2.4V
0 1 0	2.2V
0 1 1	1.8V
1 0 0	3.6V
1 0 1	2.0V
1 1 0	2.0V, Disable by Sleep
1 1 1	Disable

INTEDG: Interrupt edge select bit.

- = 0, interrupt on falling edge of INT pin.
- = 1, interrupt on rising edge of INT pin.

LVREN: LVDT reset function select bit.

- = 0, Enable LVDT reset chip, reset voltage define by LVDSSEL<2:0>.
- = 1, Disable LVDT reset chip.

IOB3EN: IOB3/RSTB function select bit.

- = 0, RSTB pin is select, IOB3 state of the bit is read as "0".
- = 1, IOB3 pin is select.

RDPORT: Read port control bit for output pins.

- = 0, From pins.
- = 1, From register.

EIS: Define the function of IOB0/INT pin.

- = 0, IOB0 (bi-directional I/O pin) is selected. The path of INT is masked.
- = 1, INT (external interrupt pin) is selected. In this case, the I/O control bit of IOB0 must be set to "1". The path of Port B input change of IOB0 pin is masked by hardware, the status of INT pin can also be read by way of reading PORTB.

2.1.11 INTEN (Interrupt Mask Register)

Read/Write-POR		R/W-0	-	-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0E	INTEN	GIE	-	-	LVDTIE	CMPIE	INTIE	RFCIE	T1IE

Legend: - = unimplemented, read as '0'.

T1IE: Timer1 overflow interrupt enable bit.

- = 0, Disable the Timer1 overflow interrupt.
- = 1, Enable the Timer1 overflow interrupt.

INTIE: External INT pin interrupt enable bit.

- = 0, Disable the External INT pin interrupt.
- = 1, Enable the External INT pin interrupt.

RFCIE: RFC module interrupt enable bit.

- = 0, Disable the RFC module interrupt.
- = 1, Enable the RFC module interrupt.

CMPIE: Comparator change interrupt enable bit.

- = 0, Disable the comparator output change interrupt.
- = 1, Enable the comparator output change interrupt.

LVDTIE: LVDT interrupt enable bit.

- = 0, Disable the LVDT falling edge interrupt.
- = 1, Enable the LVDT falling edge interrupt.

GIE: Global interrupt enable bit.

- = 0, Disable all interrupts. For wake-up from SLEEP mode through an interrupt event, the device will continue execution at the instruction after the SLEEP instruction.
- = 1, Enable all un-masked interrupts. For wake-up from SLEEP mode through an interrupt event, the device will branch to the interrupt address (0x008).

Note: When an interrupt event occurs with the GIE bit and its corresponding interrupt enable bit are all set, the GIE bit will be cleared by hardware to disable any further interrupts. The RETFIE instruction will exit the interrupt routine and set the GIE bit to re-enable interrupt.

2.1.12 INTFLAG (Interrupt Status Register)

Read/Write-POR		-	-	-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0F	INTFLAG	-	-	-	LVDTIF	CMPIF	INTIF	RFCIF	T1IF

Legend: - = unimplemented, read as '0'.

T1IF: Timer1 overflow interrupt flag. Set when TMR1 overflows, reset by software.

RFCIF: RFC module interrupt flag. Set when RFC conversion is completed if RFCMOD = 0, reset by software.

INTIF: External INT pin interrupt flag. Set by rising/falling (selected by INTEDG bit (LVDTCON<6>)) edge on INT pin, reset by software.

LVDTIF: LVDT interrupt flag. Set when V_{DD} under LVDT level, reset by software.

2.1.13 PWMCON (PWM Control Register) (BANK0 & 1)

Read/Write-POR		-	-	-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x10	PWMCON	-	-	-	PWMCS2	PWMCS1	PWMCS0	P1EN	P0EN

Legend: - = unimplemented, read as '0'.

P0EN: PWM0 module enable bit.

= 0, Disable PWM0 output, IOA1/PWM0 pin is configured to IOA1 pin.

= 1, Enable PWM0 output, IOA1/PWM0 pin is configured to PWM0 pin.

P1EN: PWM1 module enable bit.

= 0, Disable PWM1 output, IOA2/PWM1 pin is configured to IOA2 pin.

= 1, Enable PWM1 output, IOA2/PWM1 pin is configured to PWM1 pin.

PWMCS2:PWMCS0: PWM clock source select bits.

PWMCS2:PWC0	PWM1 & 2 clock source
0 0 0	HIRC * 2
0 0 1	HIRC
0 1 0	HIRC / 2
0 1 1	HIRC / 4
1 0 0	HIRC / 8
1 0 1	HIRC / 16
1 1 0	HIRC / 32
1 1 1	LIRC

2.1.14 P0DPR (PWM0 Duty compare Pre-set Register) (BANK0 & 1)

Read/Write-POR		R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x011	P0DPR	PWM0 Duty Compare Pre-set register							

P0DPR is PWM0 duty-cycle compare value pre-set register.

2.1.15 P1DPR (PWM1 Duty compare Pre-set Register) (BANK0 & 1)

Read/Write-POR		R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x012	P1DPR	PWM1 Duty Compare Pre-set register							

P1DPR is PWM1 duty-cycle compare value pre-set register.

2.1.16 RFCCON (RFC Control Register) (BANK0 & 1)

Read/Write-POR		R/W-0	R/W-0	-	R/W-0	-	-	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x013	RFCCON	RFCON	START	-	RFCMOD	-	-	RFCS1	RFCS0

Legend: - = unimplemented, read as '0'.

RFCS1:RFCS0: Select one the RFC oscillation network of RFCx (x = 0 to 2). The selected RFCx pin will be configured as output pin if RFCON = 1. Other RFCx pins will behave as tristate input pins. If RFCON = 0, all RFCx pins will behave as tristate input pins.

RFCS1:RFCS0		RFC channel
0	0	RFC0 pin is selected.
0	1	RFC1 pin is selected.
1	0	RFC2 pin is selected.
1	1	No function, don't use.

RFCMOD: RFC mode selection bit.

- = 0, Enable/disable the counter by CX signal, and the clock source of the counter is the internal system clock (Fosc).
- = 1, Enable/disable the counter by START bit, and the clock source of the counter is the CX signal.

START: RFC counter enable bit.

- = 0, Stop the RFC conversion, reset by hardware when conversion is finished or by software.
- = 1, RFC counter start to convert.

RFCON: RFC module enable bit

- = 0, Disable RFC module, all the RFCx and CX pins will behave as tristate input pins.
- = 1, Enable RFC module.

2.1.17 RFCDLB and RFCDHB (RFC Data Register Low Byte and High Byte) (BANK0 & 1)

Read/Write-POR		R-0	R-0	R-0	R-0	R-0	R-0	R-0	
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x14	RFCDLB	Low byte of 15 bit RFC conversion result							

Read/Write-POR		R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x15	RFCDHB	RFCOV	RFCD14	RFCD13	RFCD12	RFCD11	RFCD10	RFCD9	RFCD8

RFCD14:RFCD0: RFC conversion result.

RFCOV: RFC counter overflow flag. Set when RFC counter overflow, reset by RFC counter reset.

- = 0, Not overflow.
- = 1, Overflow.

2.1.18 AWUCON (PORTA Wakeup Control Register) (BANK2 & 3)

Read/Write-POR		-	-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x010	AWUCON	-	-	WUA5	WUA4	WUA3	WUA2	WUA1	WUA0

Legend: - = unimplemented, read as '0'.

WUA0: = 0, Disable the input change interrupt/wake-up function of IOA0 pin.
 = 1, Enable the input change interrupt/wake-up function of IOA0 pin.

WUA1: = 0, Disable the input change interrupt/wake-up function of IOA1 pin.
 = 1, Enable the input change interrupt/wake-up function of IOA1 pin.

WUA2: = 0, Disable the input change interrupt/wake-up function of IOA2 pin.
 = 1, Enable the input change interrupt/wake-up function of IOA2 pin.

WUA3: = 0, Disable the input change interrupt/wake-up function of IOA3 pin.
 = 1, Enable the input change interrupt/wake-up function of IOA3 pin.

WUA4: = 0, Disable the input change interrupt/wake-up function of IOA4 pin.
 = 1, Enable the input change interrupt/wake-up function of IOA4 pin.

WUA5: = 0, Disable the input change interrupt/wake-up function of IOA5 pin.
 = 1, Enable the input change interrupt/wake-up function of IOA5 pin.

2.1.19 APHCON (PORTA Pull-high Control Register) (BANK2 & 3)

Read/Write-POR		-	-	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x011	APHCON	-	-	/PHA5	/PHA4	/PHA3	/PHA2	/PHA1	/PHA0

Legend: - = unimplemented, read as '0'.

/PHA0: = 0, Enable the internal pull-high of IOA0 pin.
 = 1, Disable the internal pull-high of IOA0 pin.

/PHA1: = 0, Enable the internal pull-high of IOA1 pin.
 = 1, Disable the internal pull-high of IOA1 pin.

/PHA2: = 0, Enable the internal pull-high of IOA2 pin.
 = 1, Disable the internal pull-high of IOA2 pin.

/PHA3: = 0, Enable the internal pull-high of IOA3 pin.
 = 1, Disable the internal pull-high of IOA3 pin.

/PHA4: = 0, Enable the internal pull-high of IOA4 pin.
 = 1, Disable the internal pull-high of IOA4 pin.

/PHA5: = 0, Enable the internal pull-high of IOA5 pin.
 = 1, Disable the internal pull-high of IOA5 pin.

2.1.20 BWUCON (PORTB Wakeup Control Register) (BANK2 & 3)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x012	BWUCON	WUB7	WUB6	WUB5	WUB4	WUB3	WUB2	WUB1	WUB0

Legend: - = unimplemented, read as '0'.

WUB0: = 0, Disable the input change interrupt/wake-up function of IOB0 pin.
= 1, Enable the input change interrupt/wake-up function of IOB0 pin.

WUB1: = 0, Disable the input change interrupt/wake-up function of IOB1 pin.
= 1, Enable the input change interrupt/wake-up function of IOB1 pin.

WUB2: = 0, Disable the input change interrupt/wake-up function of IOB2 pin.
= 1, Enable the input change interrupt/wake-up function of IOB2 pin.

WUB3: = 0, Disable the input change interrupt/wake-up function of IOB3 pin.
= 1, Enable the input change interrupt/wake-up function of IOB3 pin.

WUB4: = 0, Disable the input change interrupt/wake-up function of IOB4 pin.
= 1, Enable the input change interrupt/wake-up function of IOB4 pin.

WUB5: = 0, Disable the input change interrupt/wake-up function of IOB5 pin.
= 1, Enable the input change interrupt/wake-up function of IOB5 pin.

WUB6: = 0, Disable the input change interrupt/wake-up function of IOB6 pin.
= 1, Enable the input change interrupt/wake-up function of IOB6 pin.

WUB7: = 0, Disable the input change interrupt/wake-up function of IOB7 pin.
= 1, Enable the input change interrupt/wake-up function of IOB7 pin.

2.1.21 BPHCON (PORTB Pull-high Control Register) (BANK2 & 3)

Read/Write-POR		R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x013	BPHCON	/PHB7	/PHB6	/PHB5	/PHB4	GP	/PHB2	/PHB1	/PHB0

/PHB0: = 0, Enable the internal pull-high of IOB0 pin.
= 1, Disable the internal pull-high of IOB0 pin.

/PHB1: = 0, Enable the internal pull-high of IOB1 pin.
= 1, Disable the internal pull-high of IOB1 pin.

/PHB2: = 0, Enable the internal pull-high of IOB2 pin.
= 1, Disable the internal pull-high of IOB2 pin.

GP: General purpose read/write bits.

/PHB4: = 0, Enable the internal pull-high of IOB4 pin.
= 1, Disable the internal pull-high of IOB4 pin.

/PHB5: = 0, Enable the internal pull-high of IOB5 pin.
= 1, Disable the internal pull-high of IOB5 pin.

/PHB6: = 0, Enable the internal pull-high of IOB6 pin.
= 1, Disable the internal pull-high of IOB6 pin.

/PHB7: = 0, Enable the internal pull-high of IOB7 pin.
= 1, Disable the internal pull-high of IOB7 pin.

2.1.22 CMPCON1 (Comparator Control Register1)

Read/Write-POR		-	-	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x014	CMPCON1	-	-	COUT	CINV	CINS	CM2	CM1	CM0

Legend: - = unimplemented, read as '0'.

CM2:CM0: Comparator mode select bits. See Figure 2.9 for detail description.

CM2:CM0			Comparator mode
0	0	0	Comparator Off (lowest power)
0	0	1	
0	1	0	
0	1	1	Comparator Reset (low power)
1	0	0	Multiplexed Input with CV_{REF}
1	0	1	Multiplexed Input with Bandgap
1	1	0	Comparator with CV_{REF} & Bandgap
1	1	1	Comparator with IOB7 & IOB6

CINS: Comparator input switch bit.

When CM2:CM0 = 100 or 101:
= 0, VIN- connects to CIN-.
= 1, VIN- connects to CIN+.

Other modes:
Ignore.

CINV: Comparator output polarity inversion bit.

= 0, Output not inverted.
= 1, Output inverted.

COUT: Comparator output bit.

If C1INV = 0: = 0, VIN+ < VIN-.
= 1, VIN+ > VIN-.
If C1INV = 1: = 0, VIN+ > VIN-.
= 1, VIN+ < VIN-.

2.1.23 CMPCON2 (Comparator Control Register2)

Read/Write-POR		-	-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x15	CMPCON2	-	-	CVREN	CVRR	CVR3	CVR2	CVR1	CVR0

Legend: - = unimplemented, read as '0'.

CVR3:CVR0: Comparator voltage reference (CV_{REF}) select bits.

$$\text{If CVRR} = 1 \text{ (low range): } CV_{REF} = \frac{(CVR3:CVR0) \cdot V_{DD}}{10}$$

$$\text{If CVRR} = 0 \text{ (high range): } CV_{REF} = \frac{V_{DD}}{20} + \frac{(CVR3:CVR0) \cdot V_{DD}}{20}$$

CVRR: CV_{REF} range selection bit.

= 0, High range.

= 1, Low range.

CVREN: Comparator voltage reference (CV_{REF}) module enable bit.

= 0, Disable CV_{REF} module.

= 1, Enable CV_{REF} module.

2.1.24 ACC (Accumulator)

Read/Write-POR		R/W-x							
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
N/A	ACC	Accumulator							

Accumulator is an internal data transfer, or instruction operand holding. It cannot be addressed.

2.2 I/O Ports

PORTA and PORTB are bi-directional tristate I/O ports. PORTA are 6-pin I/O port, PORTB are 8-pin I/O port. Please note that IOB3 is an input or open-drain output pin.

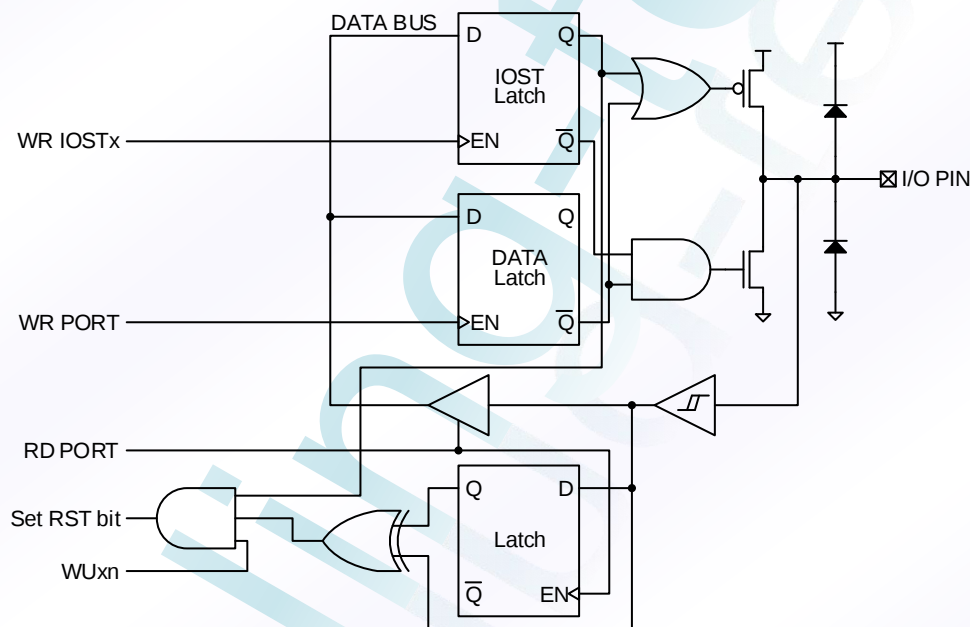
All I/O pins have data direction control registers (IOSTA, IOSTB) which can configure these pins as output or input. IOA<5:0>, IOB<5:4> and IOB<2:0> have its corresponding pull-high control bits (APHCON and BPHCON register) to enable the weak internal pull-high. The weak pull-high is automatically turned off when the pin is configured as an output pin.

All I/O pins also provides the input change interrupt/wake-up function. Each pin has its corresponding input change interrupt/wake-up enable bits (AWUCON and BWUCON) to select the input change interrupt/wake-up source. The IOB0 is also an external interrupt input signal.

Please note, IOB3 voltage on these pins must not exceed V_{DD} , otherwise it will cause the pin breakdown.

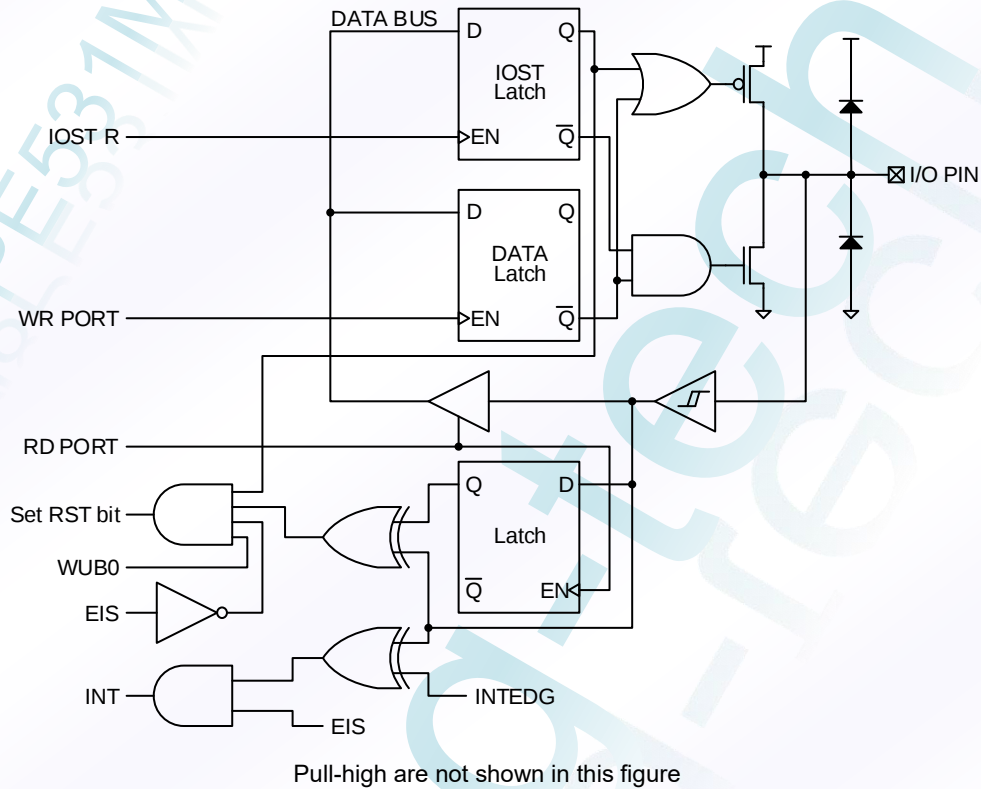
Figure 2.3: Block Diagram of I/O Pins

IOA5 ~ IOA0, IOB5, IOB4, IOB2, IOB1:

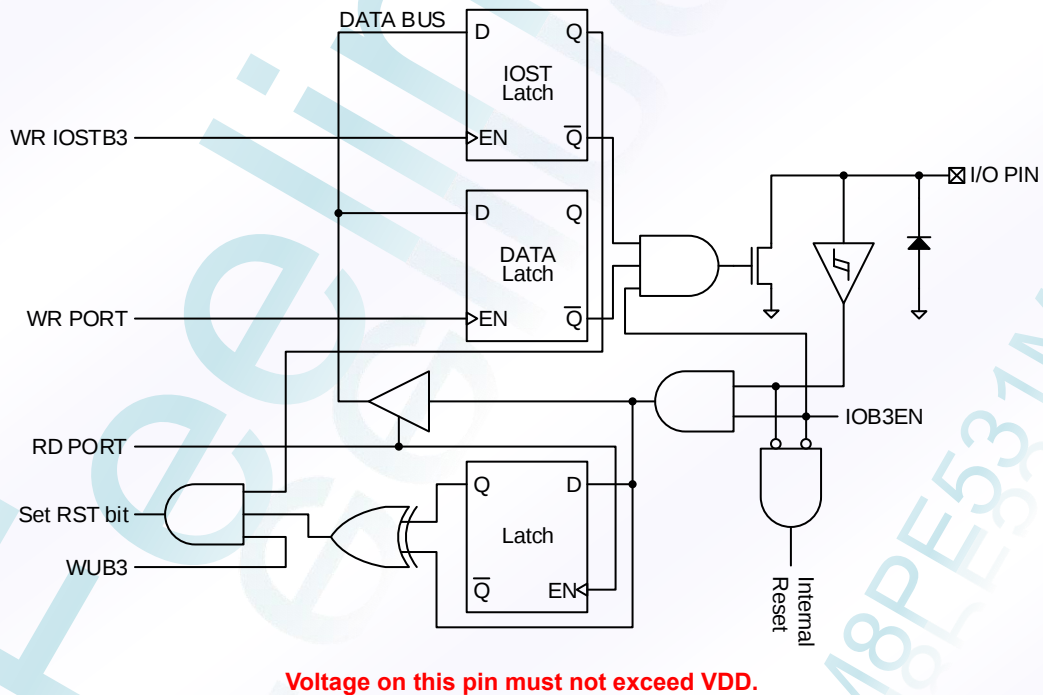


Pull-high are not shown in this figure

IOB0:



IOB3:

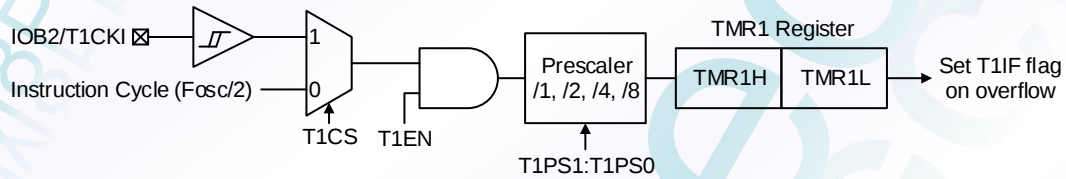


2.3 Timer1

The Timer1 is a 16-bit timer/counter with the following features:

- Readable and writable.
- Internal or external clock selection.
- Asynchronous operation.
- Interrupt on overflow from 0xFFFF to 0x0000.
- Wake-up upon overflow

Figure 2.4: Block Diagram of the Timer1



2.4 Resistor to Frequency Converter (RFC)

The Resistor to Frequency Converter (RFC) can compare three different sensors with the reference resistor separately.

This RFC contains eighteen external pins:

CX: the oscillation Schmitt trigger input (IOA3/CX pin).

RFC0 ~ RFC2: the resistor/sensor output pin 0 ~ 2 (RFC0, RFC1, and RFC2 pins)

Figure 2.5: The Block Diagram of RFC

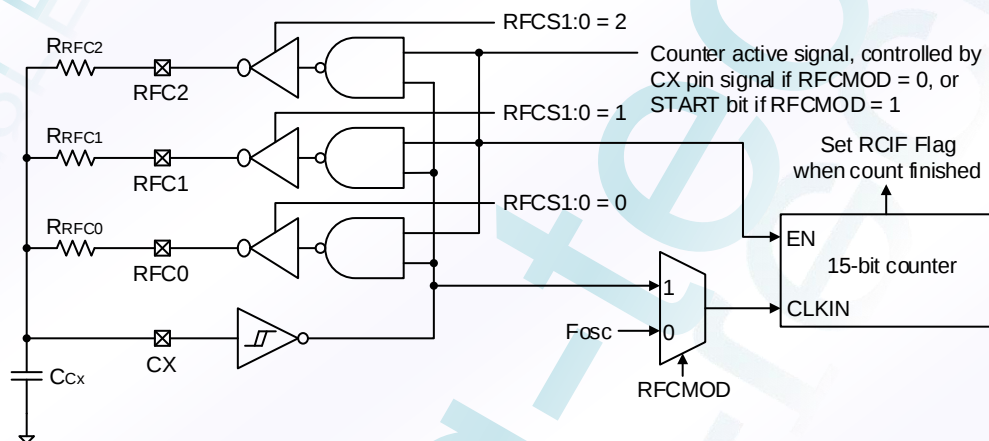


Table 2.1: The Description of RFC Control Bits

RFCS1:RFCS0	Select one the RFC oscillation network of RFCx (x = 0 to 2). The selected RFCx pin will be configured as RFCx output pin if RFCON = 1. Other RFCx pins will still behave as tristate input pins. If RFCON = 0, all RFCx pins will behave as tristate input pins.
RFCMOD	= 0, Enable/disable the counter by CX signal, and the clock source of the counter is the internal system clock (F _{osc}). = 1, Enable/disable the counter by START bit, and the clock source of the counter is the CX signal.
START	= 0, Stop the RFC conversion = 1, RFC counter start to convert. Reset by hardware after conversion is finished. Note: Don't clear START bit by software during the RFC conversion.
RFCON	= 0, Disable RFC module, all the RFCx and CX pins will behave as tristate input pins. = 1, Enable RFC module.

2.4.1 RC Oscillator Network

The RFC circuitry may build up 3 RC oscillation networks through RFC0 to RFC2 and CX pins with external resistors. Only one RC oscillation network may be active at a time. When the oscillation network is built up, the count active pulse will be generated by the oscillation network and transferred to the 15-bit counter through the CX pin. It will then enable or disable the 15-bit counter in order to count the oscillation clock. **The 15-bit RFC counter is cleared when a value is written to RFCCON register, RFCON bit is cleared, and during any kind of reset as well.**

How to build the RC oscillation network?

1. Connect the resistor and capacitor on RFCx (x = 0 to 2, if needed) and CX pins.
2. Switch all of the needed RFCx and CX pins to input mode.
3. Enable the RFC module by set the RFCON bit.
4. Select one of RFCx pins by RFCS1:RFCS0 bits to enable the output pin for RC networks respectively. The selected RFCx will output low at this time. Other RFCx pins will become of a tristate type.

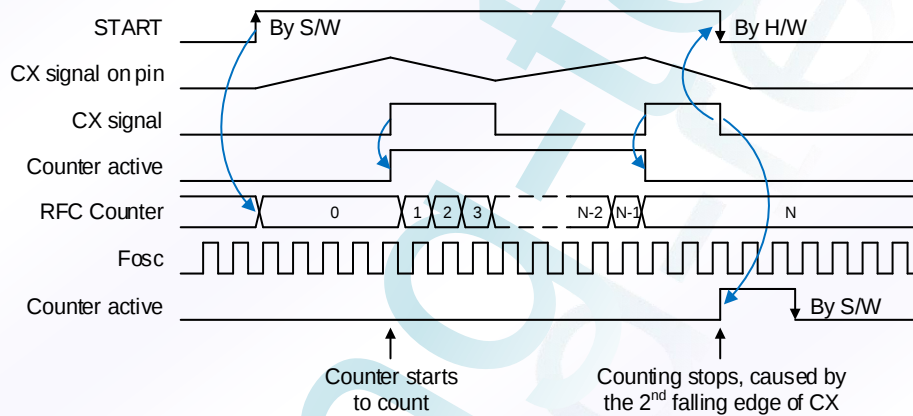
- Set START bit to enable the RC oscillation network and 15-bit counter. The RC oscillation network will not operate if this bit has not been set. Clear the START bit by H/W or S/W will finish the conversion, and the RFCIF flag will be set if RFCMOD = 0 (if enable).

2.4.2 Enable/Disable the Counter by CX Signal

In this mode, CX pin is the signal to control the counter period and the clock source of the counter comes from the internal system clock (F_{osc}).

The counter will start to count after the first rising edge signal applied on the CX pin after the RFCON bit (RFCCON<7>) is set. Once the second rising edge is applied to the CX pin after the counter is enabled, the counter will stop counting. And after the second falling edge is applied to the CX pin, the RFC block will clear the START bit and set the RFC interrupt flag RFCIF bit (RFCCON<5>) if RFCIE bit (INTEN<1>) is set. User also can be polling the RFCON or RFCIF bit to check if the conversion is finished.

Figure 2.6: The Sample of the RFC Counter Controlled by the CX Pin (RFCMOD = 0)

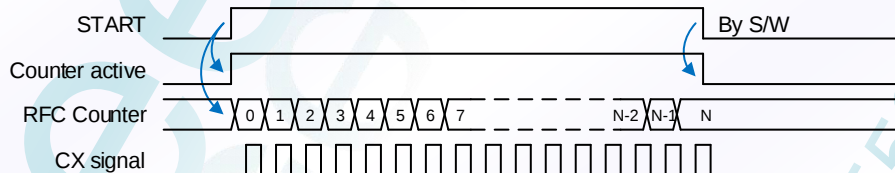


2.4.3 Enable/Disable the Counter by START Bit

In this mode, START bit is the signal to control the counter period and the clock source of the counter comes from the CX pin.

The counter will start to count after the START bit (RFCCON<6>) is set. Once the START bit is cleared by S/W, the counter will stop counting. And after the second falling edge is applied to the CX pin, the RFC block will clear the START bit and set the RFC interrupt flag RFCIF bit (INTFLAG<1>) is not needed.

Figure 2.7: The Sample of the RFC Counter Controlled by the START Bit (RFCMOD = 1)



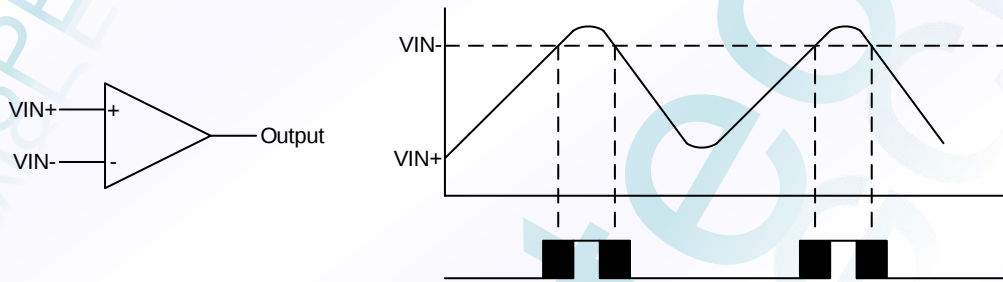
2.5 Comparator Module

The FM8PE513M device has one comparator. The inputs to the comparator 1 is multiplexed with the IOB6 and IOB7 pins. There is an on-chip comparator voltage reference (CV_{REF} and Bandgap) that can also be applied to an input of these comparators.

The compared results are stored in the COUT bit of **CMPCON1** register. This bit is read-only.

All pins configured as comparator analog inputs will read as a '0's.

Figure 2.8: Single Comparator



2.5.1 Comparator Output State

Each comparator output state can be read internally via the COUT bit of the **CMPCON1** register.

2.5.2 Comparator Output Polarity

The polarity of the comparator output can be inverted by setting the CINV bit of the **CMPCON1** register. Clearing CINV bit to "0" results in a non-inverted output. Setting CINV bit to "1" results in a polarity inverted output.

Table 2.2: COUT Status/Output vs. Input Conditions & CINV

Input Conditions	Comparator Output	CINV	COUT
$VIN+ < VIN-$	0	0	0
$VIN+ > VIN-$	1	0	1
$VIN+ < VIN-$	0	1	1
$VIN+ > VIN-$	1	1	0

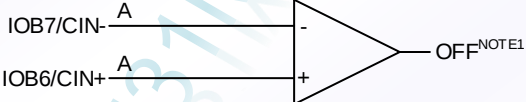
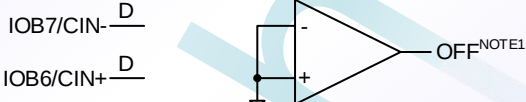
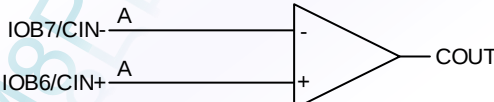
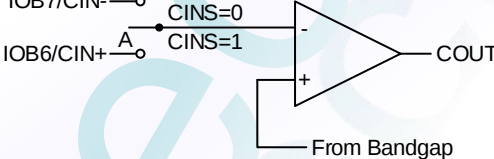
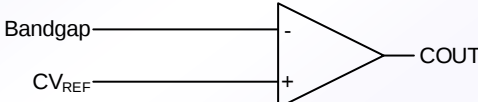
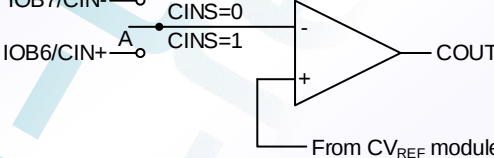
2.5.3 Comparator Input Switch

The inverting input ($VIN-$) of the comparators may be switched between two analog pins if $CM<2:0> = 100$ or 101 . In these modes, both pins remain in analog mode regardless of which pin is selected as the input. The CINS bit of the **CMPCON1** register controls the comparator input switch.

2.5.4 Comparator Operating Modes

There are six modes of operation for the comparator. The $CM<2:0>$ bits of **CMPCON1** register is used to select these modes.

Figure 2.9: Comparator I/O Operating Modes

CM2:CM0 = 011 Comparator Reset (low power) 	CM2:CM0 = 000, 001, 010 Comparator OFF (lowest power) 
CM2:CM0 = 111 Comparator with Output 	CM2:CM0 = 101 Multiplexed Input with Bandgap 
CM2:CM0 = 110 Comparator with Output 	CM2:CM0 = 100 Multiplexed Input with CVREF 

Note1: Reads as "0".

Note2: A = Comparator analog input, pins always read '0'.

CINS = Comparator input switch (CMPCON1<3>)

D = Digital I/O.

2.5.5 Comparator Voltage Reference (CVREF)

The comparator module also allows the selection of an internally generated voltage reference for one of the comparator inputs. The internal reference signal is used for four of the eight comparator modes. The CMPCON2 register controls the voltage reference module.

The voltage reference can output 32 distinct voltage levels, 16 in a high range and 16 in a low range. The following equations determine the output voltages:

$$\text{If CVRR} = 1 \text{ (low range): } CV_{REF} = \frac{(CVR3:CVR0) * V_{DD}}{18}$$

$$\text{If CVRR} = 0 \text{ (high range): } CV_{REF} = \frac{V_{DD}}{10} + \frac{(CVR3:CVR0) * V_{DD}}{20}$$

Figure 2.10: Comparator Voltage Reference

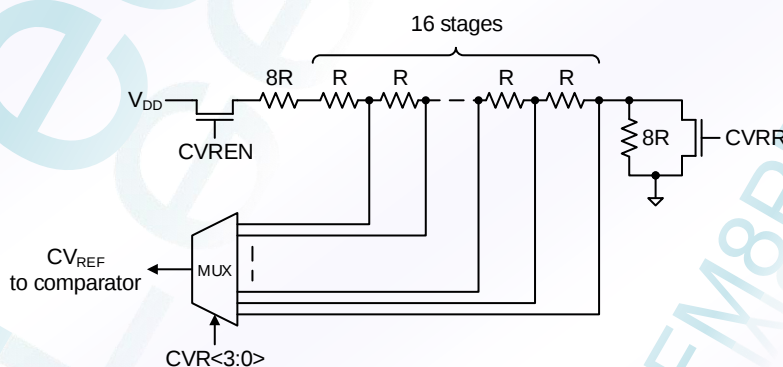


Table 2.3: Reset Conditions for All Registers

Register	Address	Power-on Reset Brown-out Reset	RSTB Reset WDT Reset
ACC	N/A	xxxx xxxx	xxxx xxxx
INDF	0x00	xxxx xxxx	uuuu uuuu
PCL	0x02	0000 0000	0000 0000
STATUS	0x03	0101 1xxx	010# #xxx
FSR	0x04	00xx xxxx	00uu uuuu
IOSTA	0x05	--11 1111	--11 1111
PORTA	0x06	--xx xxxx	--xx xxxx
IOSTB	0x07	1111 1111	1111 1111
PORTB	0x08	xxxx xxxx	xxxx xxxx
T1CON	0x09	---0 0000	---0 0000
TMR1LB	0x0A	0000 0000	0000 0000
TMR1HB	0x0B	0000 0000	0000 0000
OSCCON	0x0C	1111 0000	uuuu uuuu
LVDTCN	0x0D	1110 0111	uuuu uuuu
INTEN	0x0E	0--0 0000	0--0 0000
INTFLAG	0x0F	---0 0000	---0 0000
PWMCON	0x10, Bank0 & 1	---0 0000	---0 0000
P0DPR	0x11, Bank0 & 1	xxxx xxxx	xxxx xxxx
P1DPR	0x12, Bank0 & 1	xxxx xxxx	xxxx xxxx
RFCCON	0x13, Bank0 & 1	00-0 --00	00-0 --00
RFCDLB	0x14, Bank0 & 1	0000 0000	0000 0000
RFCDHB	0x15, Bank0 & 1	0000 0000	0000 0000
AWUCON	0x10, Bank2 & 3	--00 0000	--00 0000
APHCON	0x11, Bank2 & 3	--11 1111	--11 1111
BWUCON	0x12, Bank2 & 3	0000 0000	0000 0000
BPHCON	0x13, Bank2 & 3	1111 1111	1111 1111
CMPCON1	0x14, Bank2 & 3	--00 0000	--00 0000
CMPCON2	0x15, Bank2 & 3	--00 0000	--00 0000
General Purpose Registers	0x18 ~ 0x3F	xxxx xxxx	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented, read as 0.

= refer to the following table for possible values.

Table 2.4: RST / $\overline{TO}$ / $\overline{PD}$ Status after Reset or Wake-up

RST	$\overline{TO}$	$\overline{PD}$	RESET was caused by
0	1	1	Power-on Reset
0	1	1	Brown-out reset
0	u	u	RSTB Reset during normal operation
0	1	0	RSTB Reset during SLEEP
0	0	1	WDT Reset during normal operation
0	0	0	WDT Wake-up during SLEEP
1	1	0	Wake-up on pin change during SLEEP

Legend: u = unchanged

Table 2.5: Events Affecting $\overline{TO}$ / $\overline{PD}$ Status Bits

Event	$\overline{TO}$	$\overline{PD}$
Power-on	1	1
WDT Time-Out	0	u
SLEEP instruction	1	0
CLRWDT instruction	1	1

Legend: u = unchanged

3.0 INSTRUCTION SET

Mnemonic, Operands	Description	Operation	Cycles	Status Affected
BCR R, bit	Clear bit in R	$0 \rightarrow R$	1	-
BSR R, bit	Set bit in R	$1 \rightarrow R$	1	-
BTRSC R, bit	Test bit in R, Skip if Clear	Skip if $R = 0$	1/2	-
BTRSS R, bit	Test bit in R, Skip if Set	Skip if $R = 1$	1/2	-
NOP	No Operation	No operation	1	-
CLRWDT	Clear Watchdog Timer	$0x00 \rightarrow WDT$,	1	$\overline{TO}, \overline{PD}$
SLEEP	Go into power-down mode	$0x00 \rightarrow WDT$, $0x00 \rightarrow WDT$ pre-scaler	1	$\overline{TO}, \overline{PD}$
RETURN	Return from subroutine	Top of Stack $\rightarrow PC$	2	-
RETFIE	Return from interrupt, set GIE bit	Top of Stack $\rightarrow PC$, $1 \rightarrow GIE$	2	-
CLRA	Clear ACC	$0x00 \rightarrow ACC$	1	Z
CLRR R	Clear R	$0x00 \rightarrow R$	1	Z
MOVAR R	Move ACC to R	$ACC \rightarrow R$	1	-
MOVR R, d	Move R	$R \rightarrow dest$	1	Z
DECR R, d	Decrement R	$R - 1 \rightarrow dest$	1	Z
DECRSZ R, d	Decrement R, Skip if 0	$R - 1 \rightarrow dest$, Skip if result = 0	1/2	-
INCR R, d	Increment R	$R + 1 \rightarrow dest$	1	Z
INCRSZ R, d	Increment R, Skip if 0	$R + 1 \rightarrow dest$, Skip if result = 0	1/2	-
ADDAR R, d	Add ACC and R	$R + ACC \rightarrow dest$	1	C, DC, Z
SUBAR R, d	Subtract ACC from R	$R - ACC \rightarrow dest$	1	C, DC, Z
ADCAR R, d	Add ACC and R with Carry	$R + ACC + C \rightarrow dest$	1	C, DC, Z
SBCAR R, d	Subtract ACC from R with Carry	$R + \overline{ACC} + C \rightarrow dest$	1	C, DC, Z
ANDAR R, d	AND ACC with R	$ACC \text{ and } R \rightarrow dest$	1	Z
IORAR R, d	Inclusive OR ACC with R	$ACC \text{ or } R \rightarrow dest$	1	Z
XORAR R, d	Exclusive OR ACC with R	$R \text{ xor } ACC \rightarrow dest$	1	Z
COMR R, d	Complement R	$\overline{R} \rightarrow dest$	1	Z
RLR R, d	Rotate left R through Carry	$R<7> \rightarrow C$, $R<6:0> \rightarrow dest<7:1>$, $C \rightarrow dest<0>$	1	C
RRR R, d	Rotate right R through Carry	$C \rightarrow dest<7>$, $R<7:1> \rightarrow dest<6:0>$, $R<0> \rightarrow C$	1	C
SWAPR R, d	Swap R	$R<3:0> \rightarrow dest<7:4>$, $R<7:4> \rightarrow dest<3:0>$	1	-
MOVIA I	Move Immediate to ACC	$I \rightarrow ACC$	1	-
ADDIA I	Add ACC and Immediate	$I + ACC \rightarrow ACC$	1	C, DC, Z
SUBIA I	Subtract ACC from Immediate	$I - ACC \rightarrow ACC$	1	C, DC, Z
ANDIA I	AND Immediate with ACC	$ACC \text{ and } I \rightarrow ACC$	1	Z
IORIA I	OR Immediate with ACC	$ACC \text{ or } I \rightarrow ACC$	1	Z
XORIA I	Exclusive OR Immediate to ACC	$ACC \text{ xor } I \rightarrow ACC$	1	Z
RETIA I	Return, place Immediate in ACC	$I \rightarrow ACC$, Top of Stack $\rightarrow PC$	2	-

Mnemonic, Operands	Description	Operation	Cycles	Status Affected
CALL I	Call subroutine	PC + 1 → Top of Stack, I → PC<10:0>	2	-
GOTO I	Unconditional branch	I → PC<10:0>	2	-

Note: 1. 2 cycles for skip, else 1 cycle.

2. bit: Bit address within an 8-bit register R

R: Register address (0x00 to 0x3F)

I: Immediate data

ACC: Accumulator

d: Destination select;

=0 (store result in ACC)

=1 (store result in file register R)

dest: Destination

PC: Program Counter

WDT: Watchdog Timer Counter

GIE: Global interrupt enable bit

TO: Time-out bit

PD: Power-down bit

C: Carry bit

DC: Digital carry bit

Z: Zero bit