

HS6230 2.4G TX RF

v0.2

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Revision History

Revision	Date	Description
v0.1	2020/01/08	Initial version
v0.2	2020/07/29	Add reference design

CONTENTS

Revision History	2
1 Introduction	4
1.1 Package	4
1.2 Pin function.....	4
1.3 Reference design.....	5
2 Product Overview	6
2.1 Features.....	6
2.2 Block.....	7
2.3 Operational Modes.....	7
2.3.1 Power-Down Mode.....	8
2.3.2 Standby Modes	9
2.3.3 TX mode	9
2.3.4 Operational modes configuration.....	9
2.3.5 Timing Information.....	9
2.3.6 Air data rate	9
2.3.7 RF channel frequency	10
2.3.8 PA control	10
2.3.9 TX control.....	10
2.4 Protocol Engine	10
2.5 Protocol engine overview	11
2.6 Protocol engine packet format	11
2.6.1 Preamble	11
2.6.2 Address	11
2.6.3 Guard	11
2.6.4 Packet Control Field (PCF).....	11
2.6.5 Payload	12
2.6.6 CRC (Cyclic Redundancy Check)	12
2.6.7 Automatic packet assembly	12
2.7 Protocol engine timing.....	14
2.8 Data and control interface.....	14
2.8.1 SPI Operation.....	14
2.8.2 Data FIFO	15
2.8.3 Interrupt	15
3 Register Definition.....	16

1 Introduction

HS6230 is a 2.4 GHz ultra-low power TX RF compliant with HS6200. The RF module is configured and operated through RF register map. This register map is accessed by MCU through a 3-wire Serial Peripheral interface (SPI). HS6230 support two operation mode including 2.4G mode and BLE mode. In BLE mode, HS6230 can transmit 31 Bytes BLE broadcast packet. HS6230 need only one capacitor and one 16M crystal for peripheral circuit.

1.1 Package

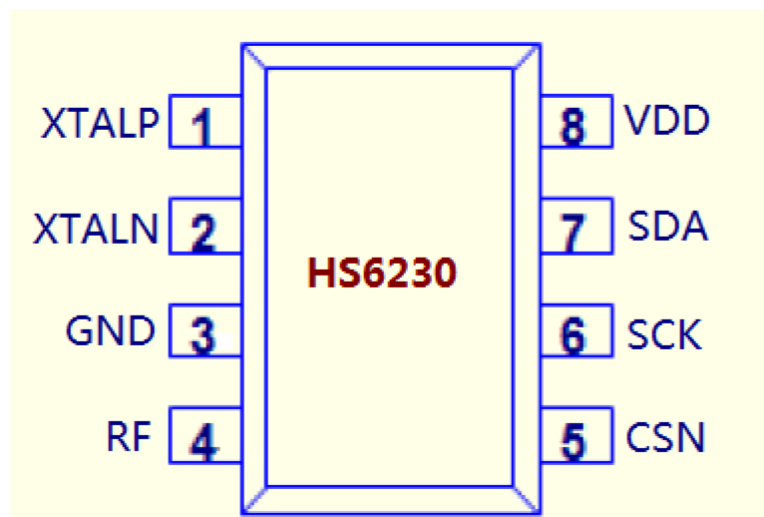


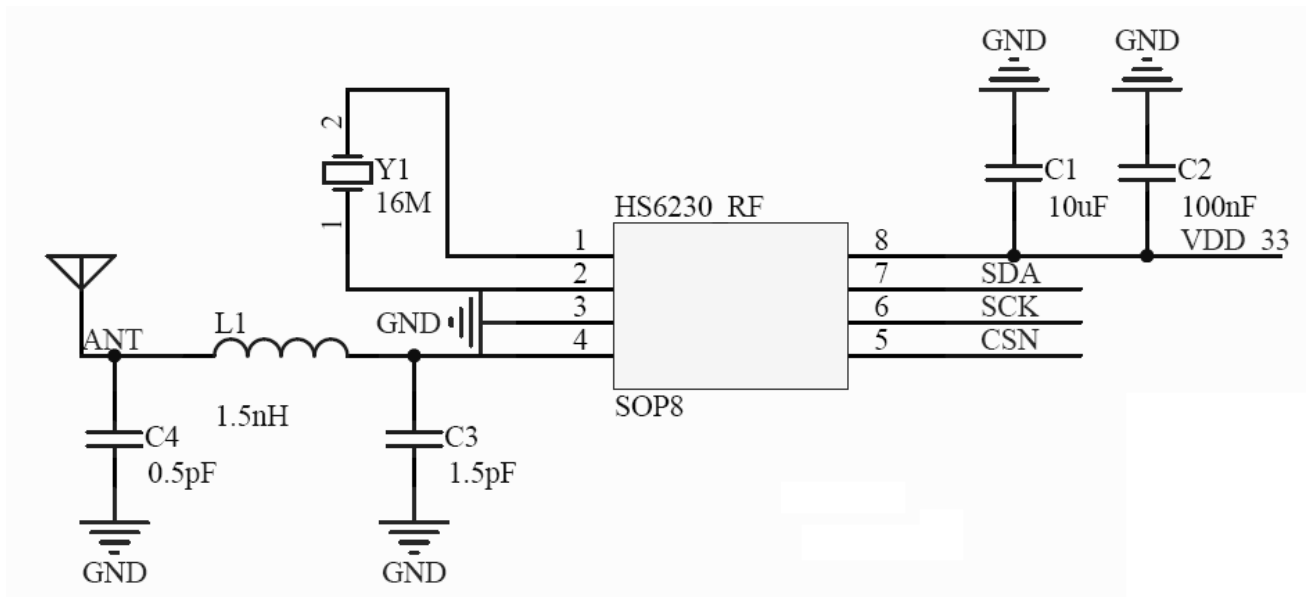
Figure1.1 HS6230 SOP8 package

1.2 Pin function

Pin No.	Pin Name	Function
1	XTALP	Crystal+
2	XTALN	Crystal-
3	GND	Ground
4	RF	Antenna
5	CSN	SPI chip select, low active
6	SCK	SPI clock
7	SDA	SPI data
8	VDD	Power, 1uF capacitor connected to VDD

Table 1.1 HS6230 SOP8 pin function

1.3 Reference design



2 Product Overview

2.1 Features

Features of HS6230 include:

- General
 - Worldwide 2.4 GHz ISM band operation
 - 1 Mbps and 250Kbps on air data rate
- Transmitter
 - Maximum output power: 12dBm
 - 17mA at 0dBm output power
 - 1.5uA at sleep mode
 - Power supply: 1.9V~3.6V
- RF Synthesizer
 - Fully integrated synthesizer
 - 1 MHz frequency programming resolution
 - Accepts low cost ± 60 ppm 16 MHz crystal
 - 1 MHz non-overlapping channel spacing at 1 Mbps
- Protocol Engine
 - 1 to 32 bytes dynamic payload length
 - Automatic packet handling (assembly)
- Interface
 - Support 3 wire and 4 wire SPI
 - Support IRQ pin

2.3 Operational Modes

The state diagrams in Figure 2.2 shows the operating modes and how they function. There are three types of distinct states highlighted in the state diagram:

- Recommended operating mode: is a recommended state used during normal operation.
- Possible operating mode: is a possible operating state, but is not used during normal operation.
- Transition state: is a time limited state used during start up of the oscillator and settling of the PLL.

Figure 2.1 RF transceiver block diagram

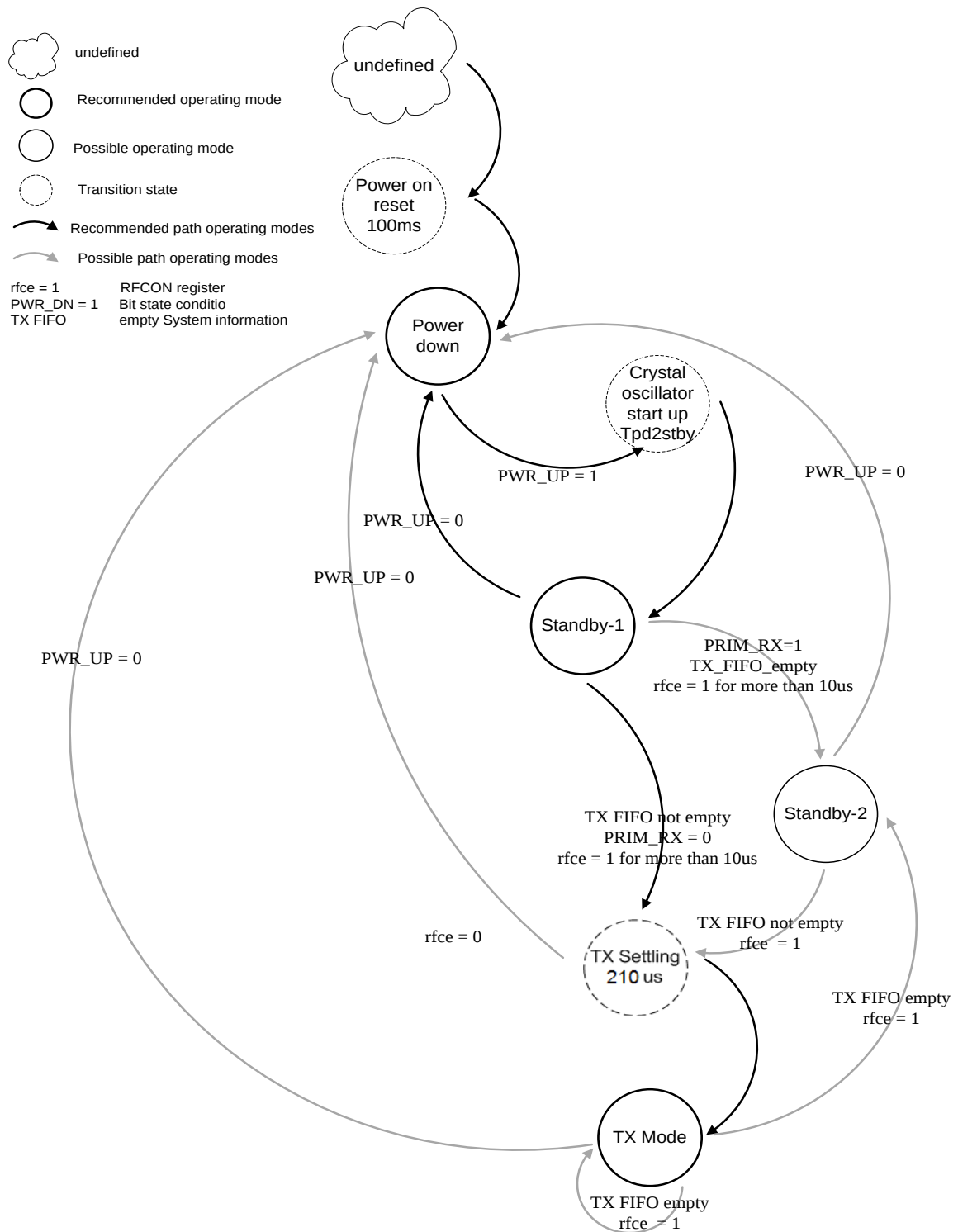


Figure 2.2 Radio control state diagram

2.3.1 Power-Down Mode

In power down mode, HS6230 is disabled using minimal current consumption. All register values available are maintained and the SPI is kept active, enabling change of configuration and the up-loading/down-loading of data registers.

2.3.2 Standby Modes

When the chip is powered up or waked up from Power-Down mode, the device enters standby mode. Standby mode is used to minimize average current consumption while maintaining short start up times. Change to TX mode only happens if CE is set high and when CE is set low, HS6230 returns to standby mode from TX mode.

2.3.3 TX mode

The TX mode is an active mode for transmitting packets. To enter this mode, the chip must have the PWR_UP bit set high, PRIM_RX bit set low, a payload in the TX FIFO and a high pulse on the CE for more than 20µs.

HS6230 stays in TX mode until it finishes transmitting a packet. If CE = 0, the chip returns to standby mode. If CE = 1, the status of the TX FIFO determines the next action. If the TX FIFO is not empty HS6230 remains in TX mode and transmits the next packet. If the TX FIFO is empty the chip goes into standby mode.

2.3.4 Operational modes configuration

The following table describes how to configure the operational modes:

Mode	PWR_UP register	PRIM_RX register	CE	FIFO state
TX mode	1	0	1	Transmit data in TX FIFO
TX mode	1	0	Minimum 20us high pulse	
Standby	1	-	-	No ongoing packet transmission
Power Down	0	-	-	-

Table 2.1 HS6230 main modes

2.3.5 Timing Information

The timing information in this section relates to the transitions between modes and the timing for the CE. The transition from standby mode to TX mode is described in Table 2.2.

Name	The chip	Max.	Min.	Comments
T _{pd2stby}	Power down→Standby mode	4ms		Time for crystal start up
T _{stby2tx}	Standby mode→TX mode		140us	
T _{hce}	Minimum CE high		20us	

Table 2.2 operational timing of the HS6230 chip

2.3.6 Air data rate

The air data rate is the modulated signaling rate the chip uses when transmitting data. It can be 250kbps or 1Mbps. Using lower air data rate gives better receiver sensitivity than higher air data rate. But, high air data rate gives lower average current consumption and

reduced probability of on-air collisions. The air data rate is set by the RF_DR bit in the RF_SETUP register. A transmitter and a receiver must be programmed with the same air data rate to communicate with each other.

2.3.7 RF channel frequency

The RF channel frequency determines the center of the channel used by the chip. The channel occupies a bandwidth of less than 1MHz at 250kbps and 1Mbps. The chip can operate on frequencies from 2.400GHz to 2.525GHz. The programming resolution of the RF channel frequency setting is 1MHz.

The RF channel frequency is set by the RF_CH register according to the following formula:

$$F0 = 2400 + \text{RF_CH [MHz]}$$

You must program a transmitter and a receiver with the same RF channel frequency to communicate with each other.

2.3.8 PA control

The PA (Power Amplifier) control is used to set the output power from the chip power amplifier. In TX mode PA control has four programmable steps, see Table 2.3.

The PA control is set by the PA_PWR bits in the RF_SETUP register.

RF-SETUP (PA_PWR)	RF output power	DC current consumption
1111	12dBm	47.5mA
1000	8dBm	28mA
0110	3dBm	21mA
0101	0dBm	17mA
0011	-6dBm	12.5mA

Conditions: VDD = 3.0V, VSS = 0V, TA = 27 °C

Table 2.3 RF output power setting for the HS6230

2.3.9 TX control

The TX control is set by PRIM_RX bit in the CONFIG register and sets the HS6230 chip in transmit mode.

2.4 Protocol Engine

Protocol engine is a packet based data link layer that features automatic packet assembly, timing and automatic acknowledgement. Protocol engine enables the implementation of ultralow power and high performance communication. The Protocol engine features enable significant improvements of power efficiency without adding complexity on the host controller side.

The main features of Protocol engine are:

- 1 to 32 bytes dynamic payload length

- Automatic packet handling

2.5 Protocol engine overview

Protocol engine uses self-defined protocol for automatic packet handling and timing. During transmit, Protocol engine assembles the packet and clocks the bits in the data packet for transmission.

2.6 Protocol engine packet format

The format of the Protocol engine packet is described in this section. The Protocol engine packet contains a preamble field, address field, packet control field, payload field and a CRC field. Figure3.3 shows the packet format with MSB to the left.

Preamble 1 byte	Address 4-5 byte	2byte guard	Packet control field 9 bit	Payload 0-32 bytes	CRC 1-2 bytes
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Figure2.3 A Protocol engine packet with payload (0-32 bytes)

2.6.1 Preamble

The preamble is a bit sequence used to synchronize the receivers demodulator to the incoming bit stream. The preamble is one byte long and is either 01010101 or 10101010. If the first bit in the address is 1 the preamble is automatically set to 10101010 and if the first bit is 0 the preamble is automatically set to 01010101. This is done to ensure there are enough transitions in the preamble to stabilize the receiver.

2.6.2 Address

This is the address for the receiver. An address ensures that the packet is detected and received by the correct receiver, preventing accidental cross talk between multiple HS6230 systems. You can configure the address field width in the AW register to be 5 bytes or 4 bytes address.

2.6.3 Guard

Figure 2.3 shows the format of the 2 bytes guard packet has better synchronous characteristics. HS6230 can bypass the 2 bytes guard by setting the register guard_en=0.

2.6.4 Packet Control Field (PCF)

Figure 2.4 shows the format of the 9 bit packet control field, MSB to the left.

Payload length 6bit	PID 2bit	NO_ACK 1bit
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Figure 2.4 Packet control field (PCF)

The packet control field contains a 6 bit payload length field, a 2 bit PID (Packet Identity) field and a 1 bit NO_ACK flag.

Note: For detailed description, please see HS6200 datasheet.

2.6.5 Payload

The payload is the user defined content of the packet. It can be 0 to 32 bytes wide and is transmitted on-air when it is uploaded to the device.

Protocol engine provides two alternatives for handling payload lengths; static and dynamic.

The default is static payload length. With static payload length all packets between a transmitter and a receiver have the same length. Static payload length is set by the RX_PW_Px registers on the receiver side. The payload length on the transmitter side is set by the number of bytes clocked into the TX_FIFO and must equal the value in the RX_PW_Px register on the receiver side.

Dynamic Payload Length (DPL) is an alternative to static payload length. DPL enables the transmitter to send packets with variable payload length to the receiver. This means that for a system with different payload lengths it is not necessary to scale the packet length to the longest payload.

In order to enable DPL the EN_DPL bit in the FEATURE register must be enabled.

2.6.6 CRC (Cyclic Redundancy Check)

The CRC is the error detection mechanism in the packet. It may either be 1 or 2 bytes and is calculated over the address, Packet Control Field and Payload.

The polynomial for 1 byte CRC is $X^8 + X^2 + X + 1$. Initial value 0xFF.

The polynomial for 2 byte CRC is $X^{16} + X^{12} + X^5 + 1$. Initial value 0xFFFF.

The number of bytes in the CRC is set by the CRCO bit in the CONFIG register. No packet is accepted by protocol engine if the CRC fails.

2.6.7 Automatic packet assembly

The automatic packet assembly assembles the preamble, address, packet control field, payload and CRC to make a complete packet before it is transmitted.

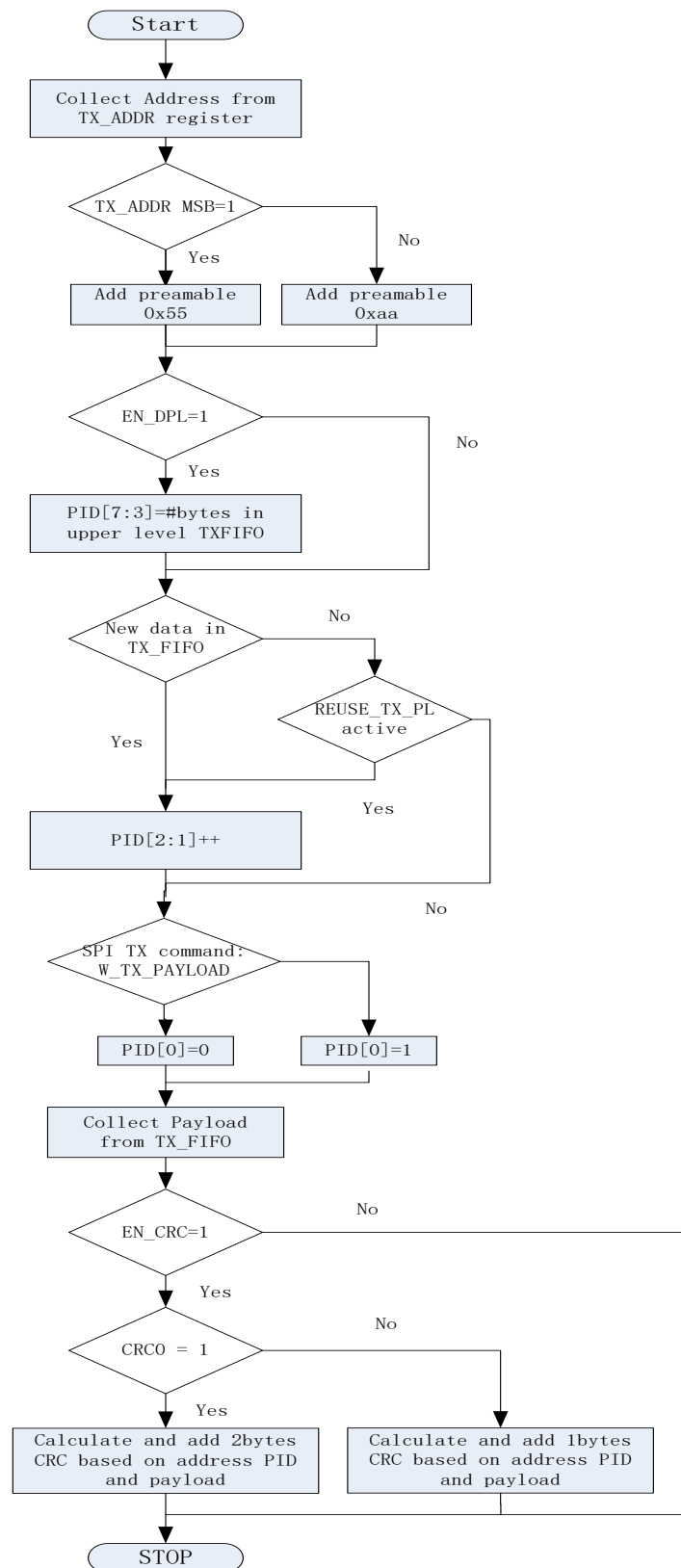


Figure 2.5 Automatic packet assembly

2.7 Protocol engine timing

This section describes the timing sequence of Protocol engine and how all modes are initiated and operated. The Protocol engine timing is controlled through the Data and Control interface. The RF transceiver can be set to static modes or autonomous modes where the internal state machine controls the events. Each autonomous mode/sequence ends with a RFIRQ interrupt. All the interrupts are indicated as IRQ events in the timing diagrams.

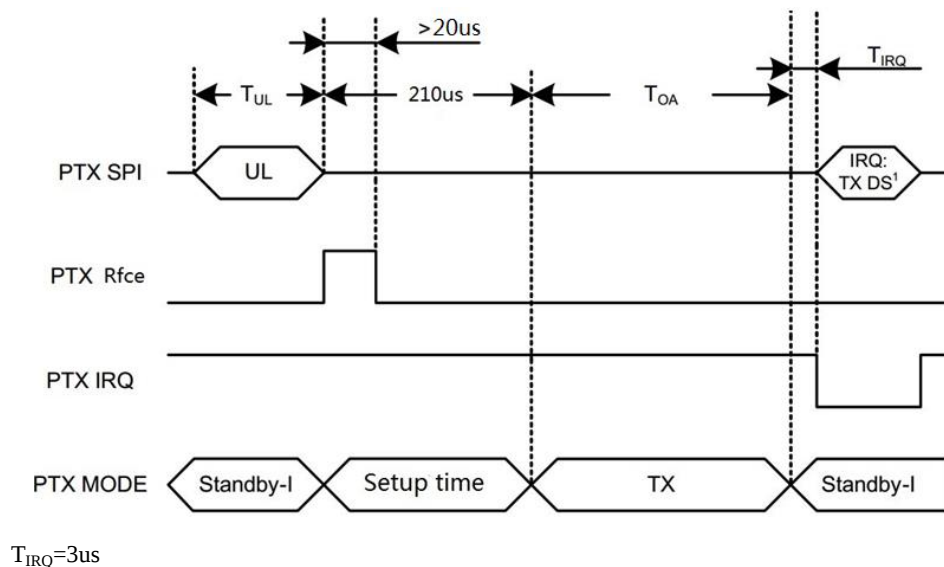


Figure 2.6 Transmitting one packet with NO_ACK on

2.8 Data and control interface

The data and control interface gives you access to all the features in the HS6230. The data and control interface consists of the following six digital signals:

IRQ (this signal is active low and controlled by three maskable interrupt sources)

CE (this signal is active high and used to activate the chip in TX mode, can be replaced by register)

CSN (SPI signal)

SCK (SPI signal)

SDA (SPI signal)

2.8.1 SPI Operation

This section describes the SPI commands and timing. The SPI commands are shown in Table 2.5. Every new command must be started by writing 0 to CSN.

The serial shifting SPI commands is in the following format:

<**Command word:** MSBit to LSBit (one byte)>

<**Data bytes:** MSBit in each byte first>

Command	Command	#Data bytes	Operation
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	word (binary)		
R_RESISTER	000A AAAA	1 to 5 LSByte first	Read command and status registers. AAAA=5 bit register map address
W_RESISTER	001A AAAA	1 to 5 LSByte first	Read command and status registers. AAAA=5 bit register map address Executable in power down or standby modes only.
W_TX_PAYLOAD	1010 0000	1 to 32 LSByte first	Write TX-payload: 1 – 32 bytes. A write operation always starts at byte 0 used in TX payload.
FLUSH_TX	1110 0001	0	Flush TX FIFO, used in TX mode
NOP	1111 1111	0	No Operation. Might be used to read the STATUS register

Table2.5 Command set for the HS230 SPI

The W_REGISTER and R_REGISTER commands operate on single or multi-byte registers. When accessing multi-byte registers read or writes to the MSBit of LSByte first. You can terminate the writing before all bytes in a multi-byte register are written, leaving the unwritten MSByte(s) unchanged.

2.8.2 Data FIFO

HS6230 has 1 level 32 bytes data FIFO which is accessible through the SPI by using dedicated SPI commands. You can write to the TX FIFO using the commands of W_TX_PAYLOAD. You can read if the TX FIFO are full or empty in the FIFO_STATUS register.

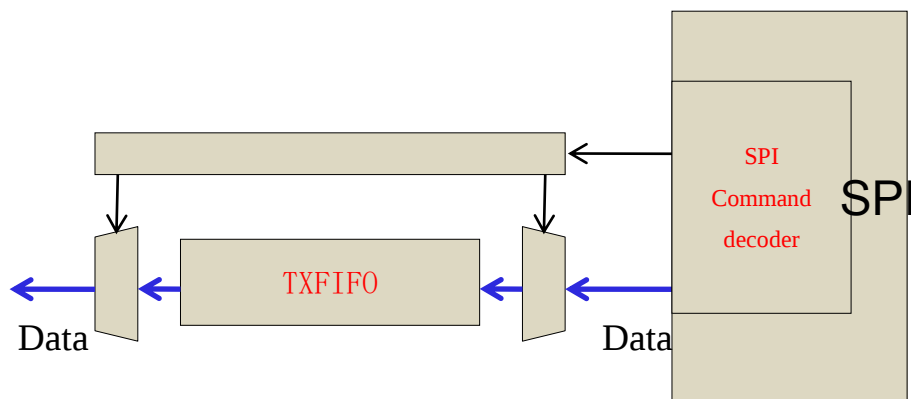


Figure 2.7 FIFO (TX) block diagram

2.8.3 Interrupt

HS6230 can send interrupts to the MCU. The interrupt (IRQ) is activated when TX_DS is set high by the state machine in the STATUS register. IRQ is deactivated when the MCU writes '1' to the interrupt source bit in the STATUS register. The interrupt mask in the CONFIG register is used to select the IRQ sources that are allowed to activate IRQ. By setting one of the mask bits high, the corresponding interrupt source is disabled. By default all interrupt sources are enabled.

3 Register Definition

Please see HS6230 RF Register Map v0.8.pdf